


CB-3 LOGIC SCHEMATICS

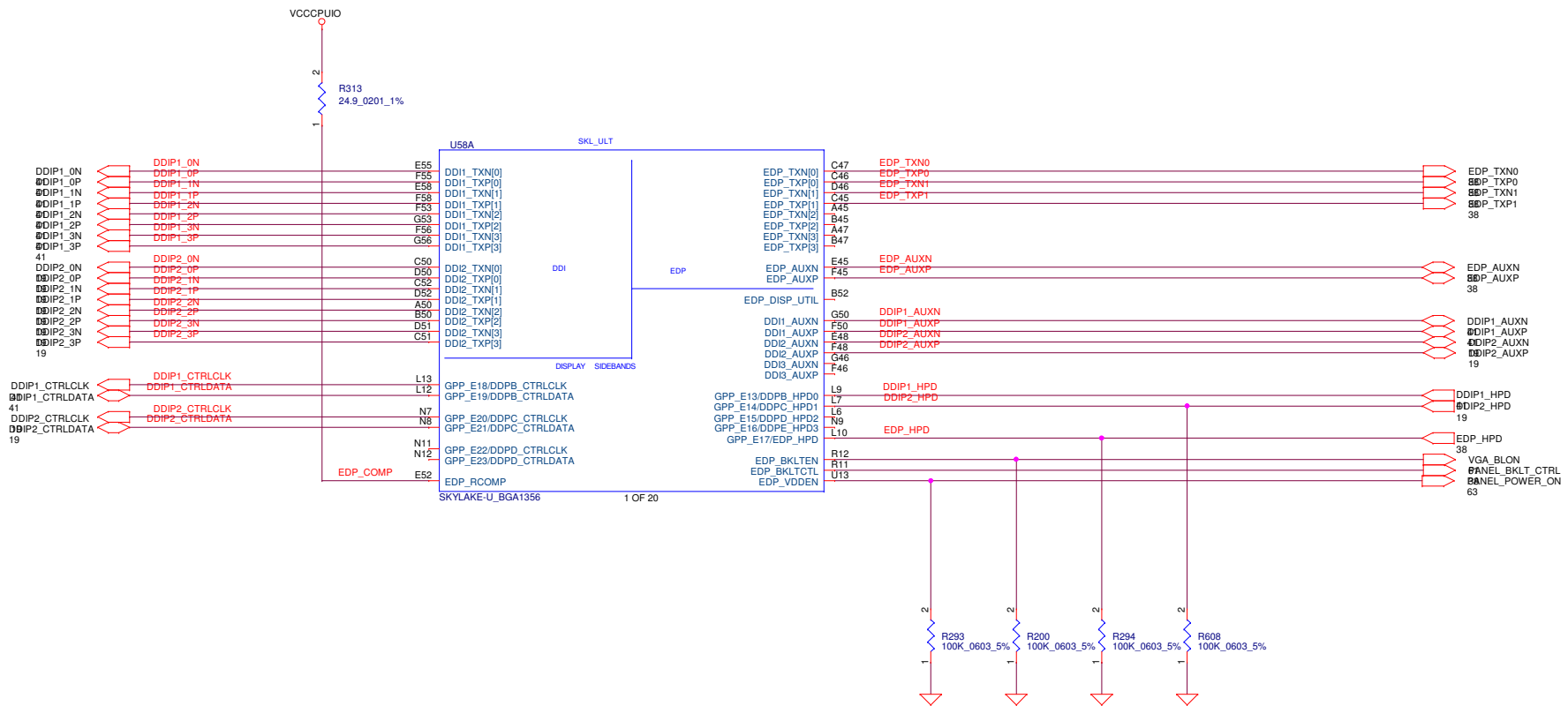
001.TITLE PAGE	36.MEMORY TERMINATION	
002.EC HISTORY	37.BLANK	
003.CPU(1/16) : DDI/EDP	38.LCD CONNECTOR	
004.CPU(2/16) : MISC/JTAG	39.BLANK	
005.CPU(3/16) : DDR3L CHANNEL-A	40.EXT CRT INTERFACE	
006.CPU(4/16) : DDR3L CHANNEL-B	41.DISPLAY PORT CONNECTOR	71.THINK ENGINE(1/2)
007.CPU(5/16) : RTC/HDA/SATA/JTAG	42.BLANK	72.THINK ENGINE(2/2)
008.CPU(6/16) : CLOCK SIGNALS	43.SATA HDD CONN	73.DC-IN
009.CPU(7/16) : LPC/SPI/SMBUS/C-LINK	44.BLANK	74.BATTERY INPUT
010.CPU(8/16) : SYSTEM PM	45.USB POWER/CONN	75.BATTERY CHARGER(BQ24760)
011.CPU(9/16) : LCD/PCI/DDI CONTROL	46.GBE CLARKVILLE	76.CHARGER SELECTOR
012.CPU(10/16) : GPIO/CPU/MISC/LPIO	47.BLANK	77.BATTERY MONITOR
013.CPU(11/16) : PCIE/USB	48.GBE MAGNETICS	78.DC/DC VCC5M/VCC3M (TPS51220A)
014.CPU(12/16) : POWER	49.RJ45 CONNECTOR	79.DC/DC VCCCPUCORE(VT1328M)
015.CPU(13/16) : POWER	50.PCIE MINI CARD SLOT	80.DC/DC VCCCPUCORE(VT1334S)
016.CPU(14/16) : GND	51.MEDIA CARD CONTROLLER	81.BLANK
017.CPU(15/16) : NCTF	52.MEDIA CARD INTERFACE	82.VCCCPUCORE DECOUPLING
018.CPU(16/16) : CFG/RESERVED	53.SMART CARD I/F	83.DC/DC VCCGFXCORE_D (TPS51728)
019.DDI-VGA CONVERTER	54.AUDIO ALC3232-GR	84.BLANK
020.BLANK	55.AUDIO CONNECTOR	85.DC/DC VCC1R05AMT(VT356)
021.XDP CONNECTOR	56.AUDIO JACK SENSE	86.DC/DC VCC1R35A(VT357)
022.RTC BATTERY	57.AUDIO EXT MIC I/F	87.DC/DC VCC0R675B(TPS51200)
023.SPI FLASH	58.AUDIO SPEAKER	88.DC/DC VCC1R5VIDEO(VT356)
024.DDR3L SO DIMM CHANNEL-A	59.AUDIO BEEP	89.DC/DC VCC1R05VIDEO_PLL(BD3551HFN)
025.BLANK	60.BLANK	90.DC/DC VCC1R8B(BD9139)
026.DDR3L SO DIMM CHANNEL-B	61.MEC1619(1/3)	91.BLANK
027.DDR3L DECOUPLING	62.MEC1619(2/3)	92.DC/DC VCC1R5B(BD3551HFN)
028.N15S-GM(1/6) : PEG I/F	63.MEC1619(3/3)	93.LOAD SW PCH SUS
029.N15S-GM(2/6) : DIGITAL OUT I/F	64.KEYBOARD CONNECTOR	94.LOAD SW LAN
030.N15S-GM(3/6) : VRAM I/F	65.TOUCH PAD CONNECTOR	95.LOAD SW VIDEO
031.N15S-GM(4/6) : GPIO	66.BLANK	96.LOAD SW B
032.N15S-GM(5/6) : POWER	67.FAN CONNECTOR	97.BLANK
033.N15S-GM(6/6) : GND	68.G-SENSOR	98.LOAD SW WWAN & WLAN
034.VRAM CHANNEL-A	69.TPM	99.PTH FOR SCREW HOLES
035.BLANK	70.EEPROM/SMBUS SW	100.3rd USB

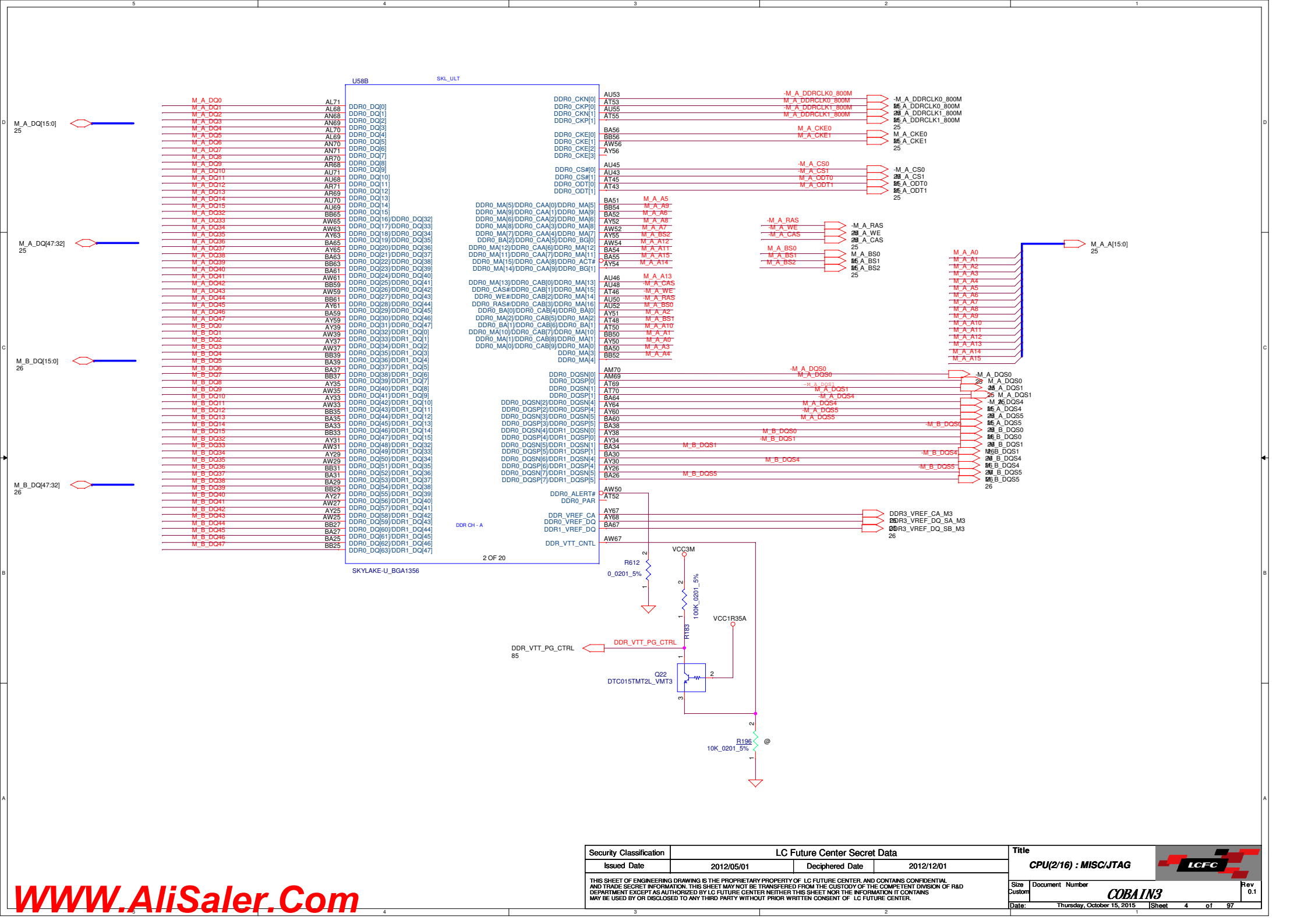
EC Modify History

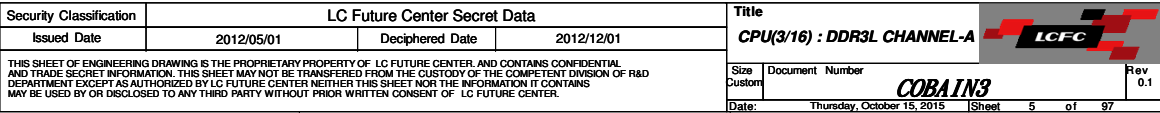
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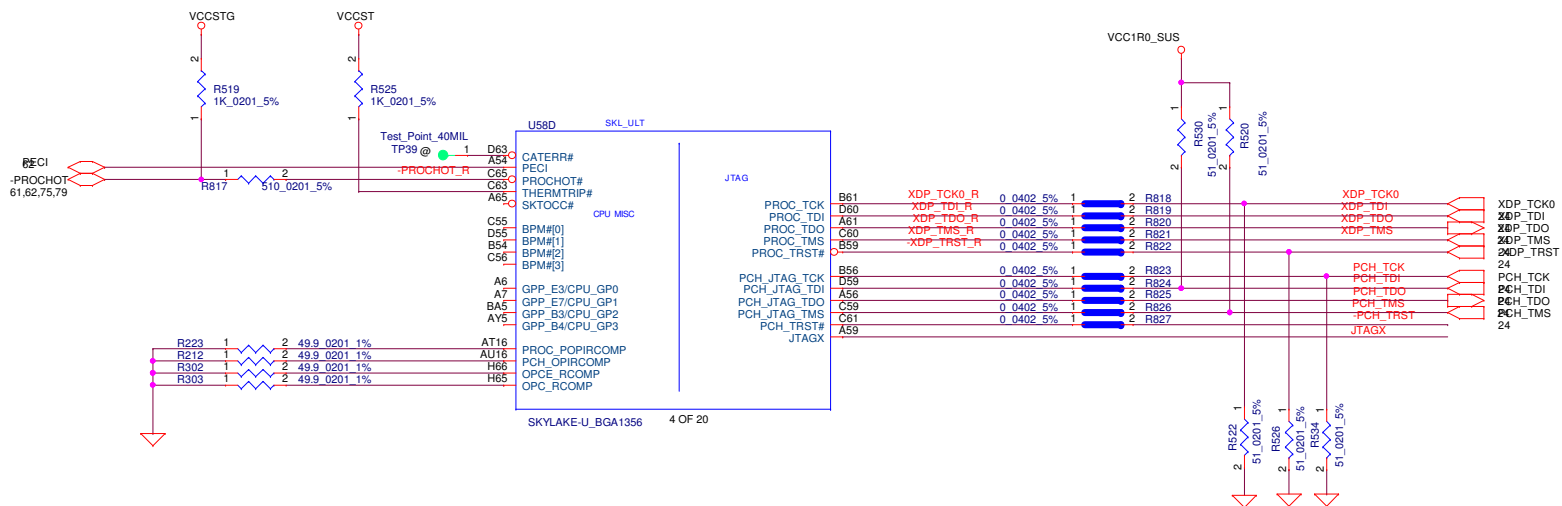
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2012/10/09	CB_1_SWG_SDV_EC011	JV_CB-1_SWG_SDV1_SCH_EC009-010_100801.pdf
2012/10/12	CB_1_SWG_SDV_EC012	JV_CB-1_SWG_SDV1_SCH_EC010-011_101101.pdf
2012/10/13	CB_1_SWG_SDV_EC013	JV_CB-1_SWG_SDV1_SCH_EC011-012_101201.pdf
2012/10/16	CB_1_SWG_SDV_EC014	JV_CB-1_SWG_SDV1_SCH_EC013_101501.pdf
2012/10/17	CB_1_SWG_SDV_EC015	JV_CB-1_SWG_SDV1_SCH_EC014_101601.pdf
2012/10/18	CB_1_SWG_SDV_EC016	JV_CB-1_SWG_SDV1_SCH_EC015_101701.pdf
2012/10/19	CB_1_SWG_SDV_EC017	JV_CB-1_SWG_SDV1_SCH_EC016_101801.pdf
2012/10/20	CB_1_SWG_SDV_EC018	JV_CB-1_SWG_SDV1_SCH_EC017_101901.pdf
2012/10/25	CB_1_SWG_SDV_EC018-022	JV_CB-1_SWG_SDV1_SCH_EC018-021_102401.pdf
2012/10/31	CB_1_SWG_SDV_EC023	JV_CB-1_SWG_SDV1_SCH_EC022_103001.pdf
2012/10/32	CB_1_SWG_SDV_EC023-025	JV_CB-1_SWG_SDV1_SCH_EC023-024_103101.pdf
2012/11/15	CB_1_SWG_SDV_EC025-033	JV_CB-1_SWG_SDV1_SCH_EC025-035_112201.pdf
2012/11/23	CB_1_SWG_SDV_EC033-036	JV_CB-1_SWG_SDV1_SCH_EC036_112601.pdf
2012/11/27	CB_1_SWG_SDV_EC037	JV_CB-1_SWG_SDV1_SCH_EC037-038_120401.pdf
2012/12/05	CB_1_SWG_SDV_EC037-039	

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Issued Date		2012/05/01	Deciphered Date		2012/12/01	
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				Size	Document Number	Rev
				Quater	COBAN2 SWG	0.1
				Date:	Thursday, October 16, 2015	Sheet 2 of 97









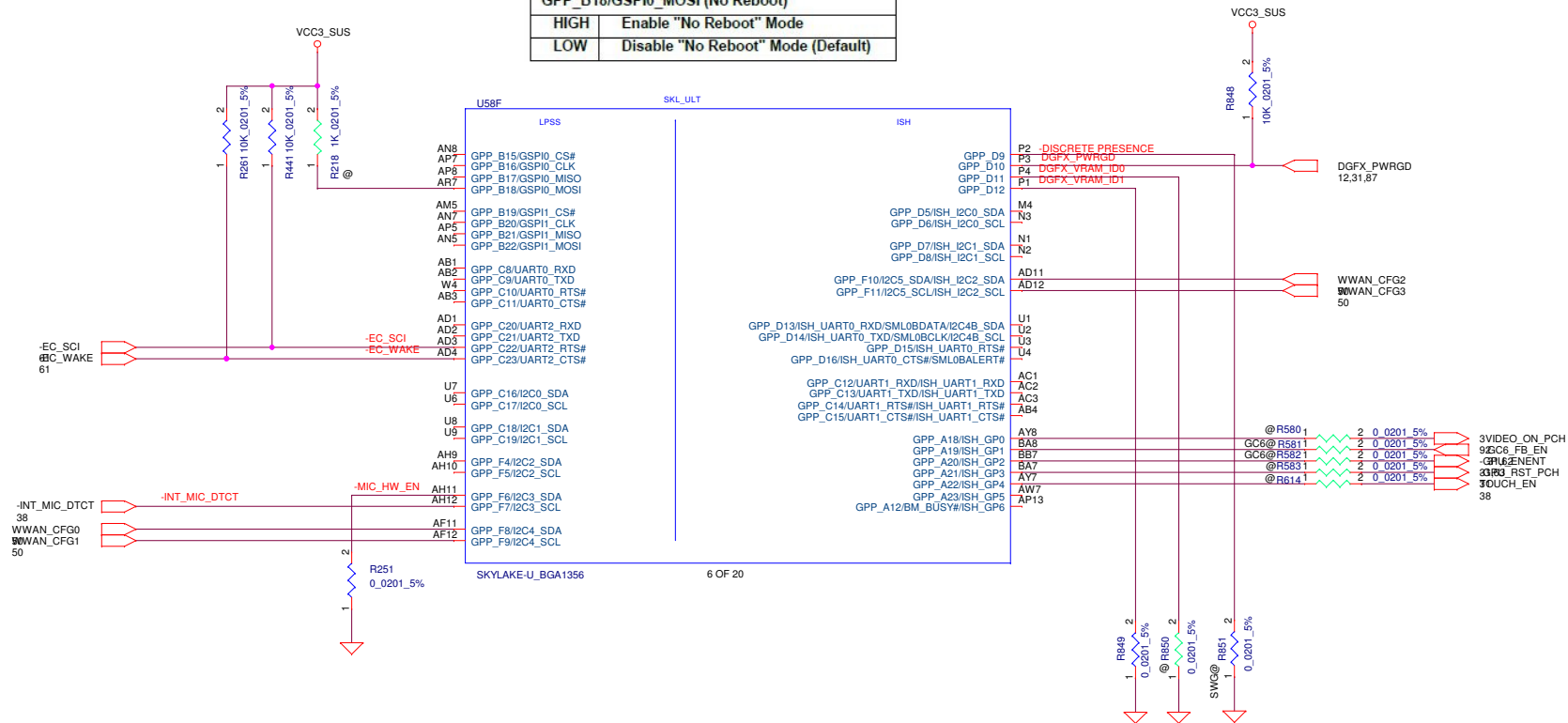
PCH_TCK	@ R538	1	2	0.0201 5%	XDP_TCK1	XDP_TCK1
PCH_TDI	@ R535	1	2	0.0201 5%	XDP_TDI	24
PCH_TDO	@ R523	1	2	0.0201 5%	XDP_TDO	
PCH_TMS	@ R521	1	2	0.0201 5%	XDP_TMS	
-PCH_TRST	@ R531	1	2	0.0201 5%	-XDP_TRST	
JTAGX	@ R536	1	2	0.0201 5%	XDP_TCK0	

TABLE : Functional Strap

GPP_B22/GSPI1_MOSI (Boot BIOS Destination)	
HIGH	Boot BIOS from LPC
LOW	Boot BIOS from SPI (Default)

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)



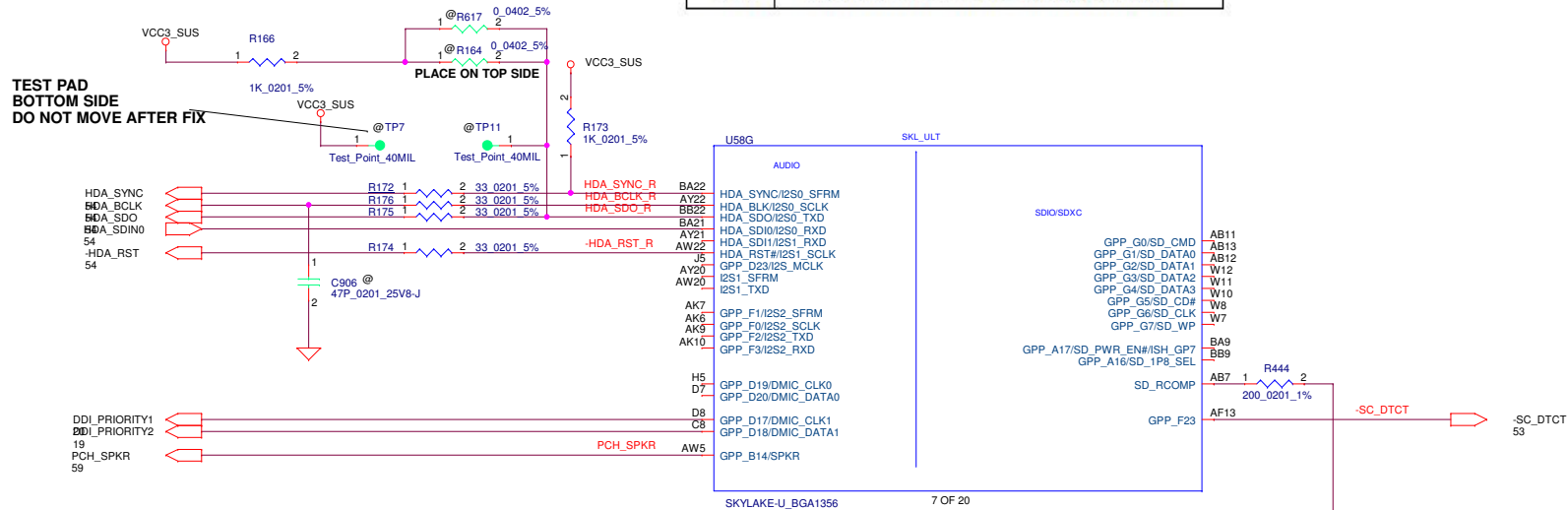
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Title		
CPU(6/16) : LPSS/ISH		
Size	Document	Number
Custom	COBAN3	
Date	Friday, October 16, 2015	Sheet 8 of 97
Rev	0.1	



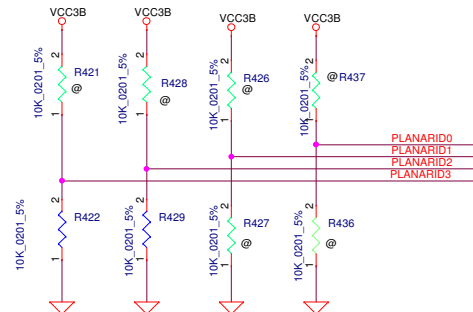
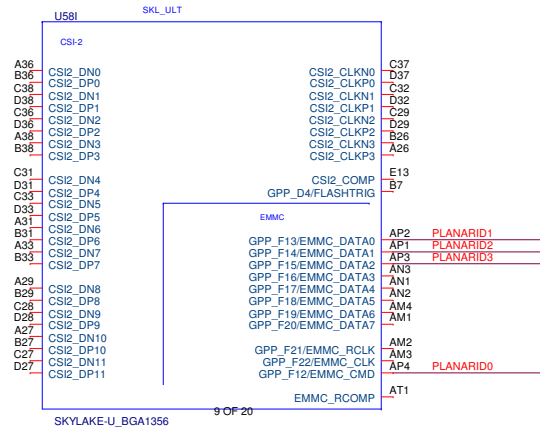
TABLE : Functional Strap

HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

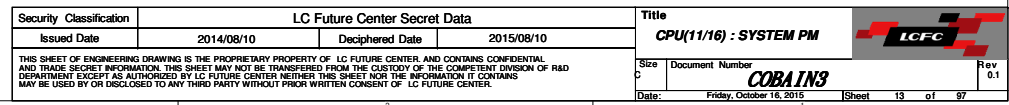


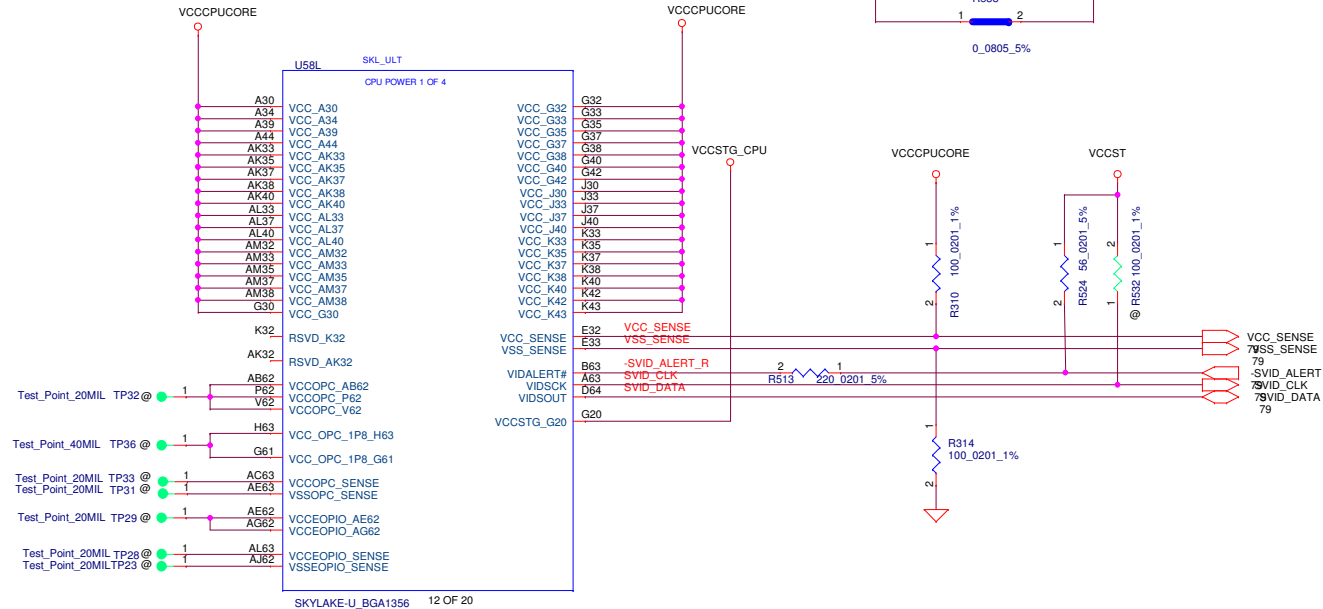
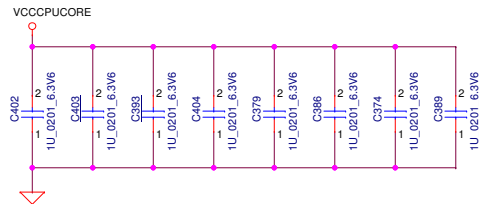
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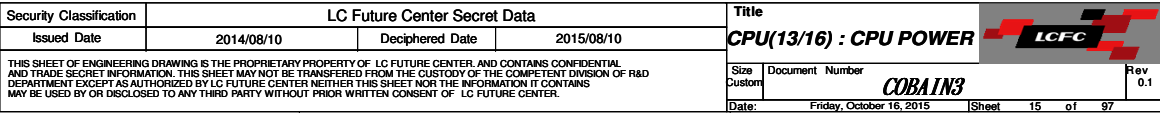
Title		LCFC	
CPU(7/16) : AUDIO/SDXC			
Size	Document Number	Rev	
Custom	COBAN3	0.1	
Date:	Thursday, October 15, 2015	Sheet	9 of 97

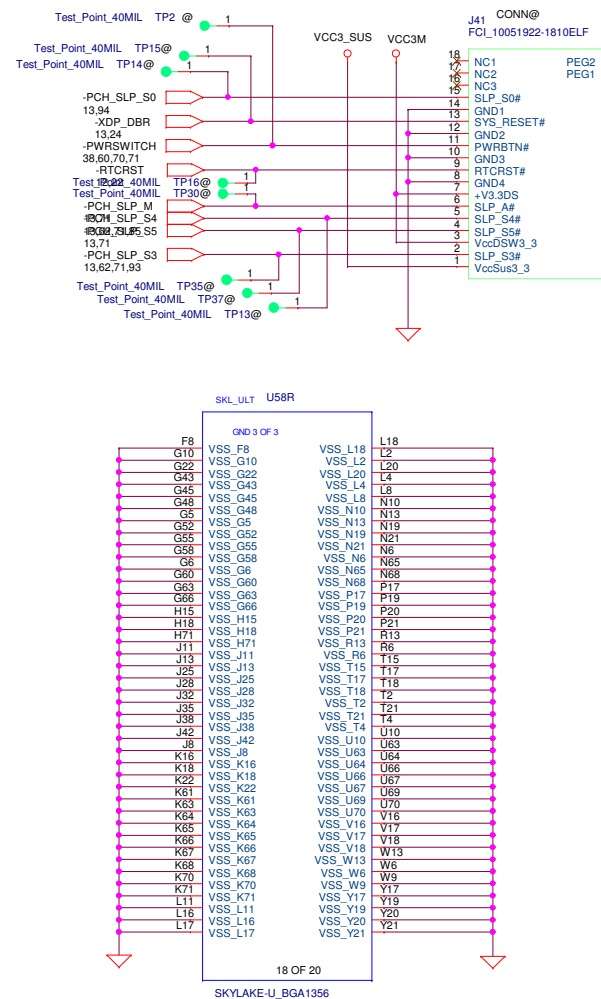
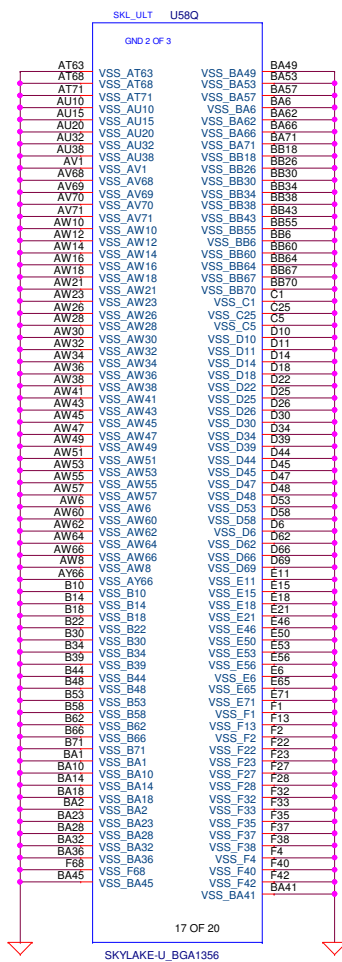
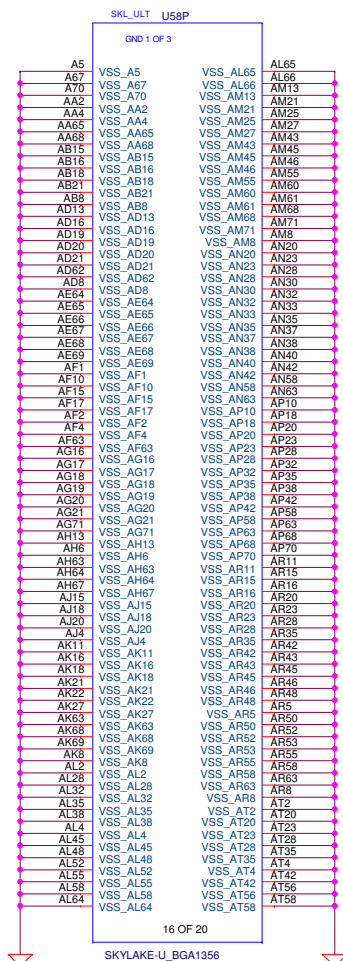


PLANAR ID TABLE		
LEVEL		PLANARID[3..0]
UMA	SWG	
SDV		0000B
FVT		0001B
SIT	FVT	0010B
SVT	SIT	0011B
	SVT	0100B





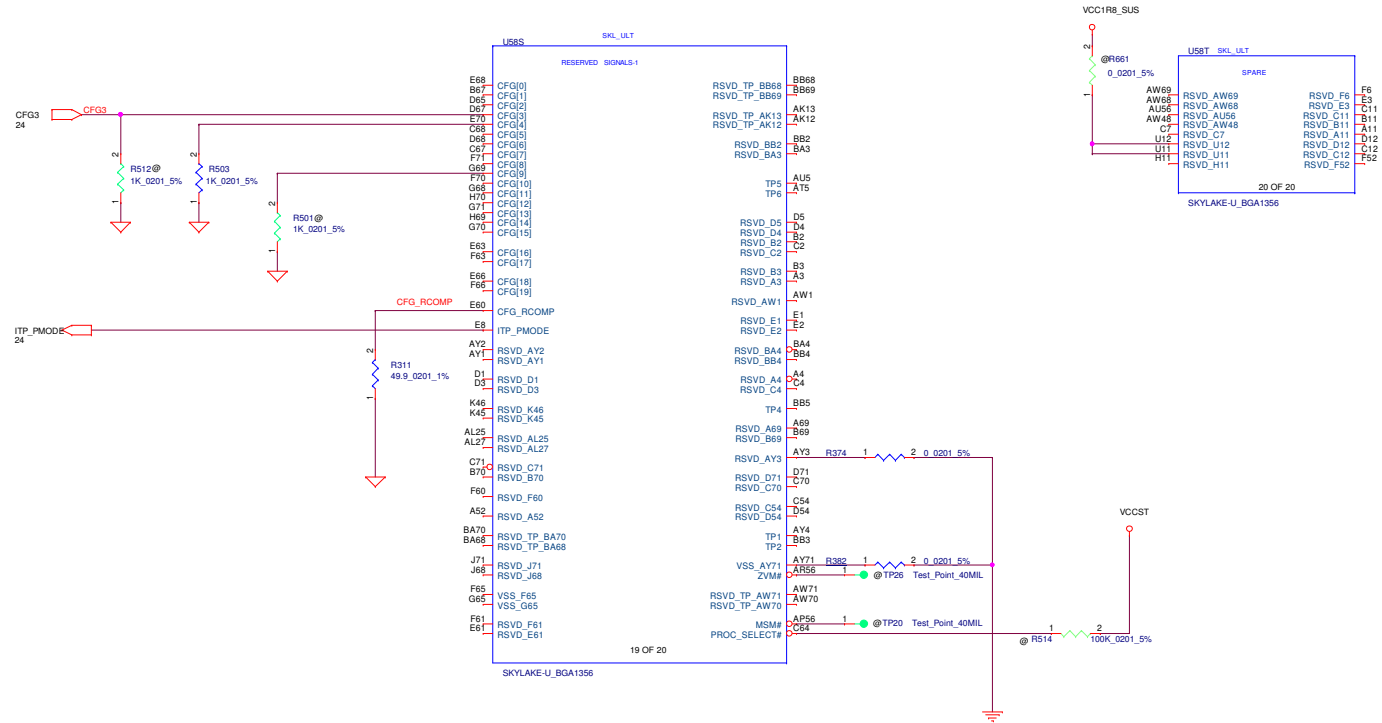




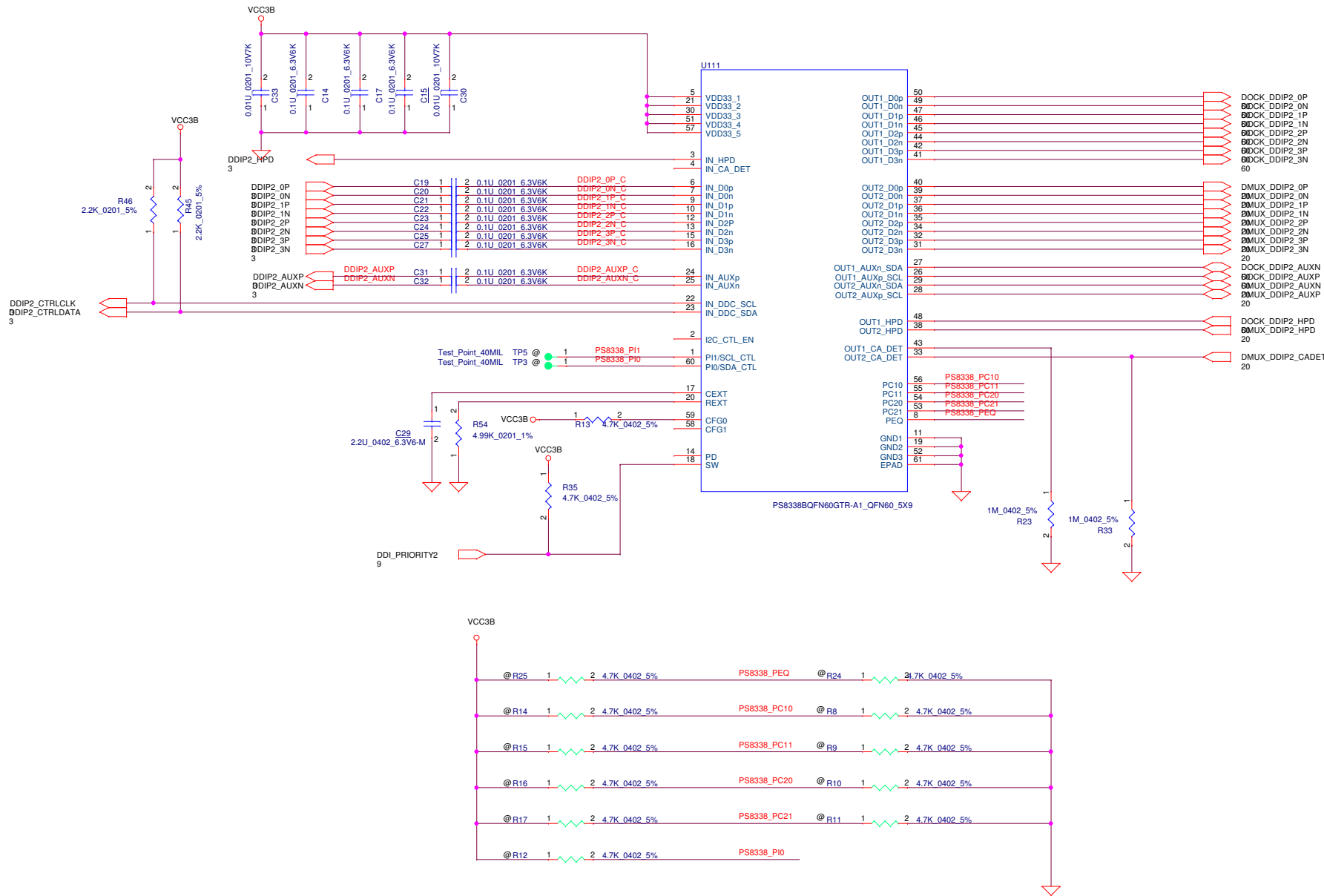
CONNECTOR	Planar Only	BOX
J41	ASM	NO ASM

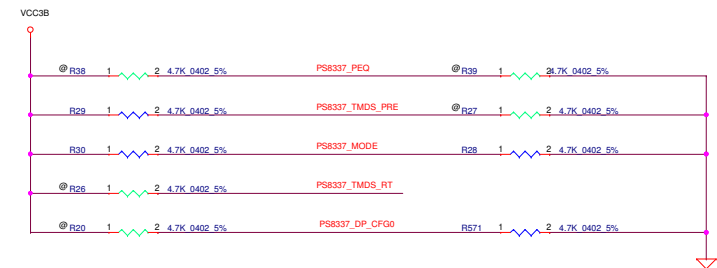
TABLE


CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted 1 : No Stall 0 : Stall
CFG4 : eDP Enable 1 : Disabled 0 : Enabled
CFG9 : SVID Bus Communication 1 : Enabled 0 : Disabled




Security Classification	LC Future Center Secret Data		Title	CPU(16/16) : CFG/RESERVED	
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Date:	Friday, October 18, 2015	Sheet	18	of	97

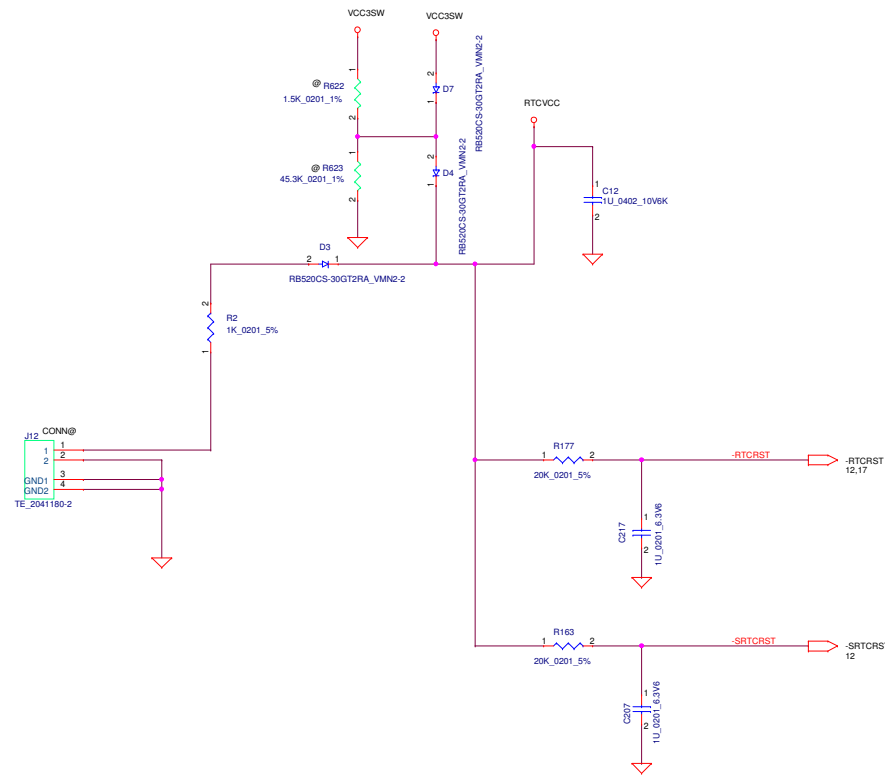





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Date		Friday, October 16, 2015		Sheet		20		of 97	

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						COBAIN3	Rev 1.0
Date:		Thursday, October 15, 2015		Sheet 21 of 97			



Security Classification				LC Future Center Secret Data				Title		
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Date:		Friday, October 18, 2015				Sheet		22	of	97



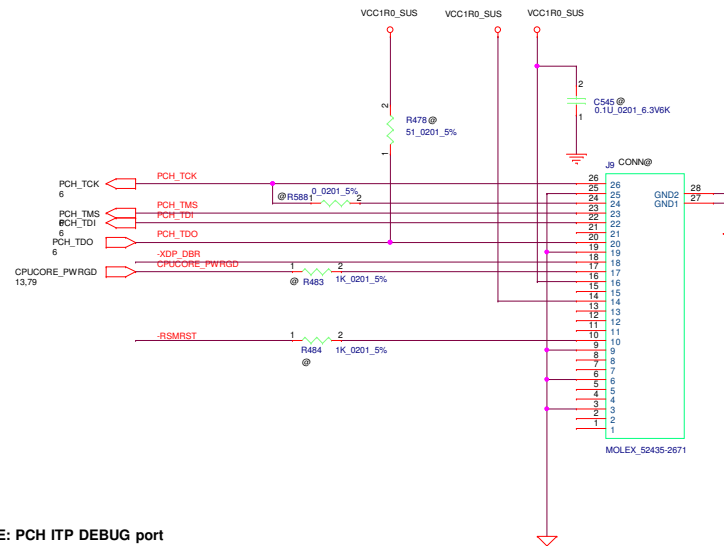
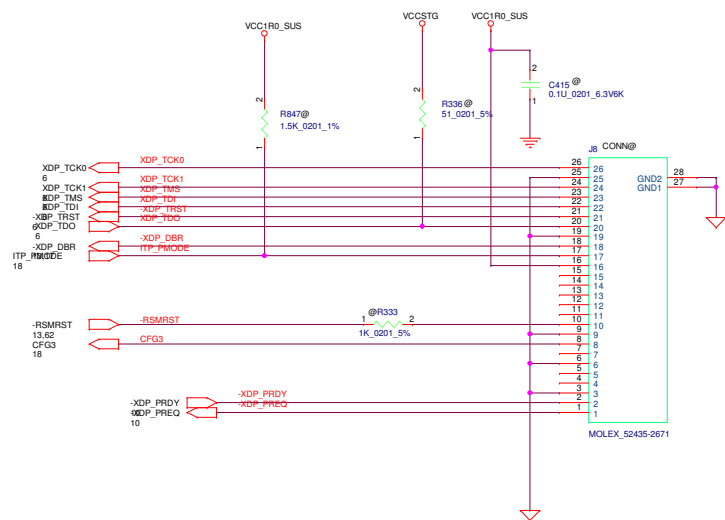

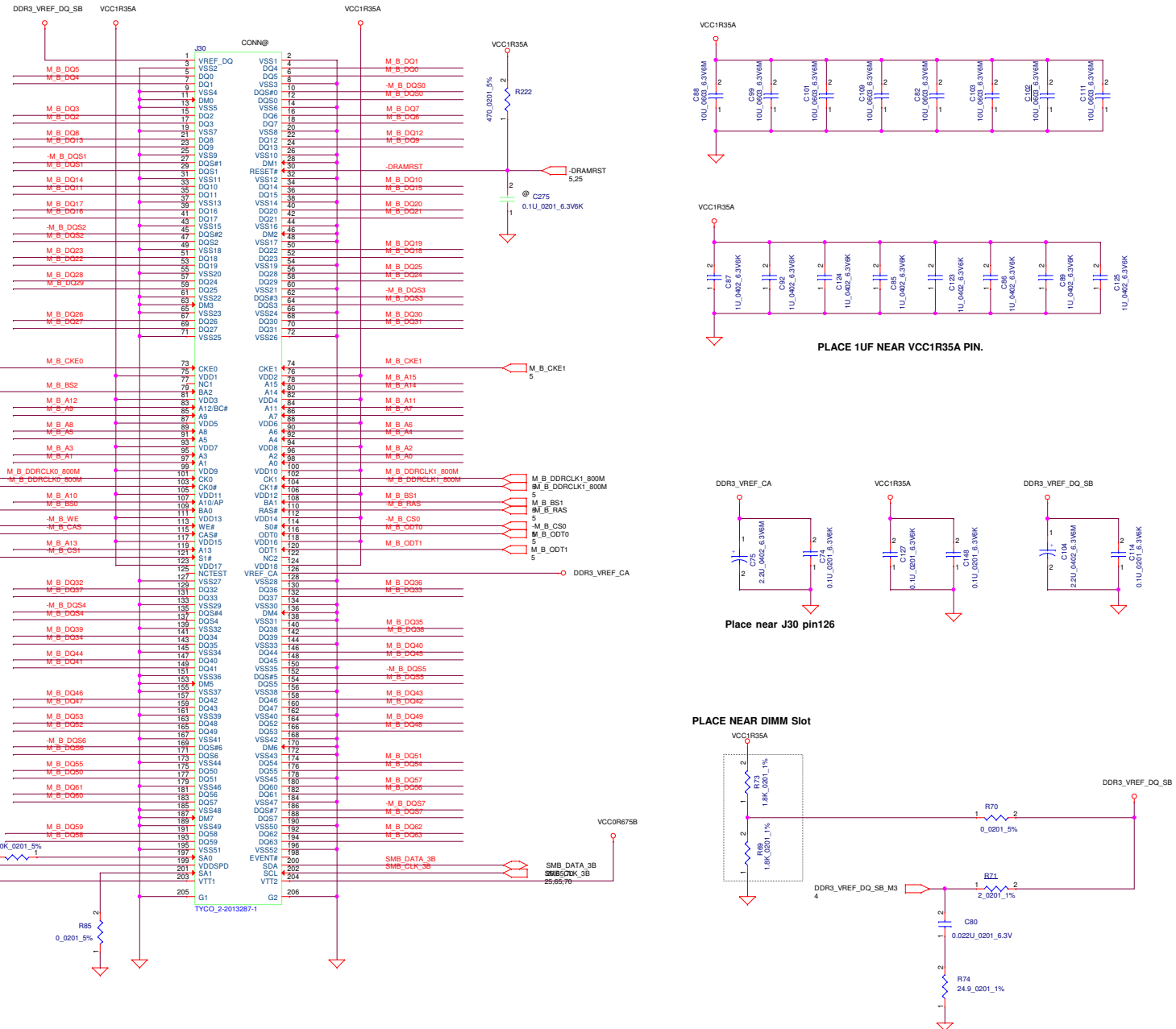
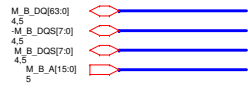


TABLE: PCH ITP DEBUG port

SIGNAL	REF DES	Planar only	BOX
TDO	R478 R523	ASM ASM	ASM ASM
TMS	R521	ASM	ASM
TDI	R535	ASM	ASM
TCK	R588 R538	ASM ASM	ASM ASM
CPUCORE_PWRGD	R483	ASM	ASM
-RSMRST	R484	ASM	ASM
CONNECTOR	J9	ASM	NO ASM

NOTE: APPLY EACH LOGIC ACCORDING TO CONFIGURATION IN SDV

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Issued Date	2012/06/21	Deciphered Date	2012/06/21	XDP CONNECTOR	
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Date:	Monday, October 15, 2018	Sheet	24	of	97





PLACE 1UF NEAR VCC1R35A PIN.

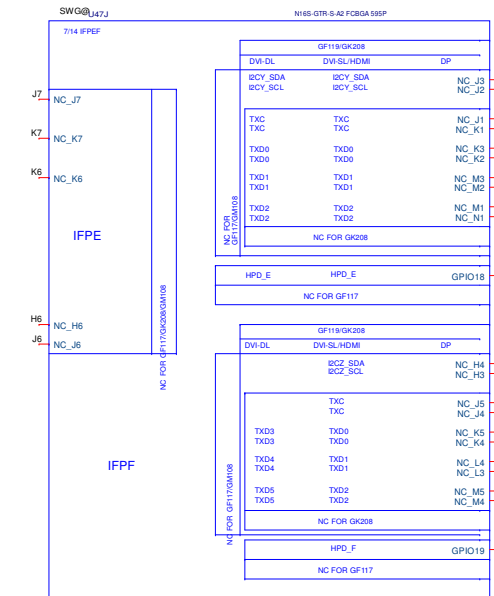
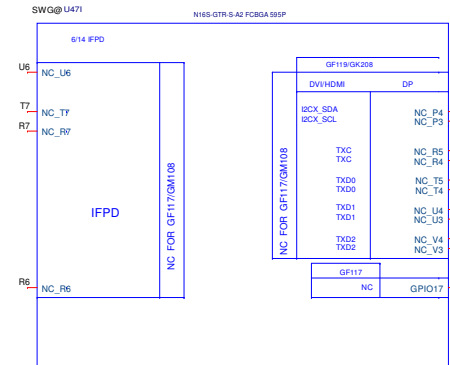
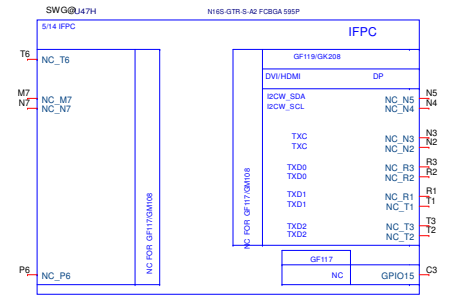
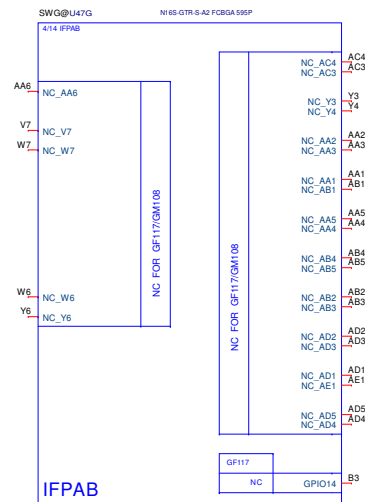
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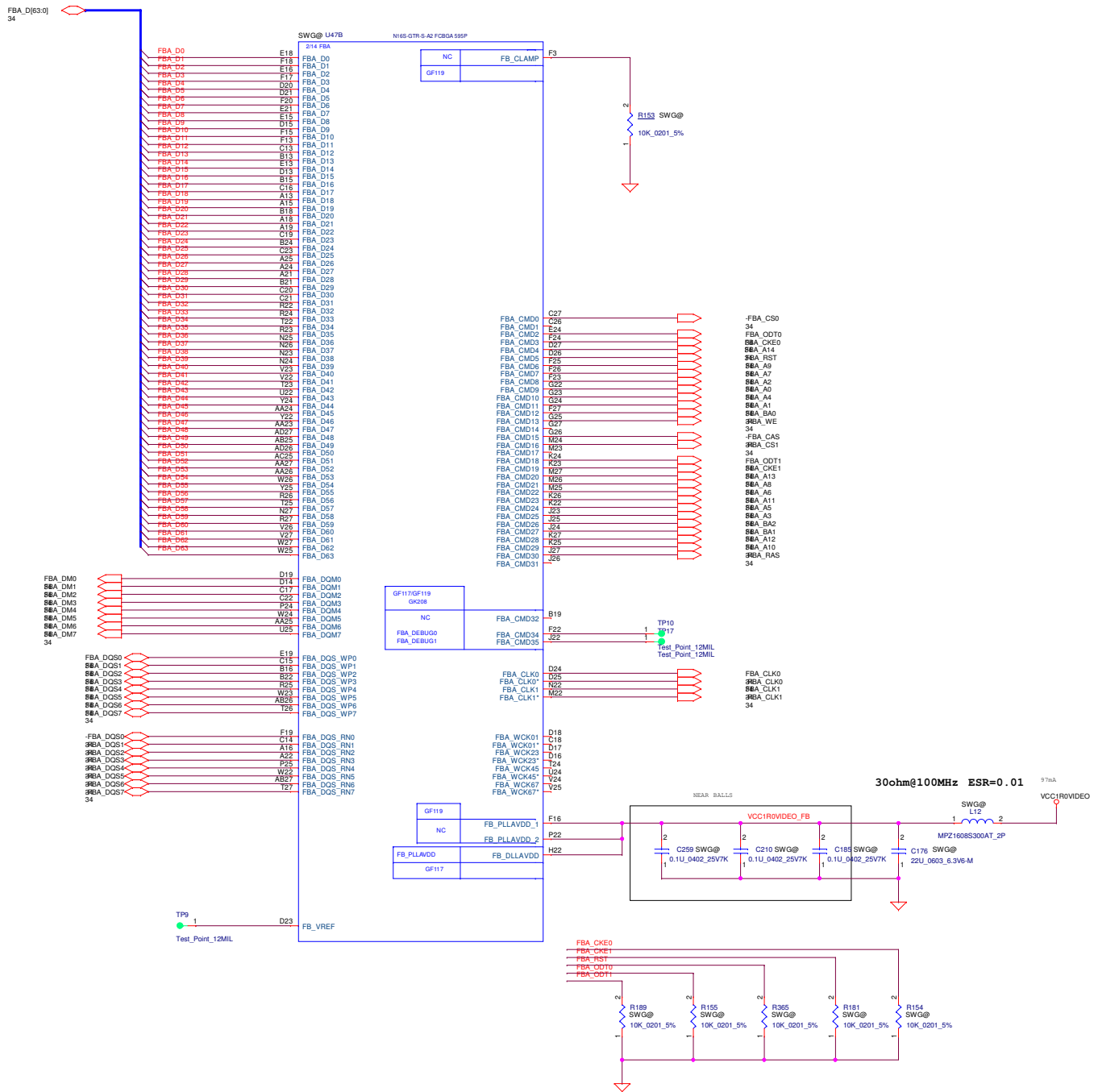
PLACE NEAR DIMM Slot

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Revision	0.1	Date	Monday, October 15, 2012
Sheet	26	of	97

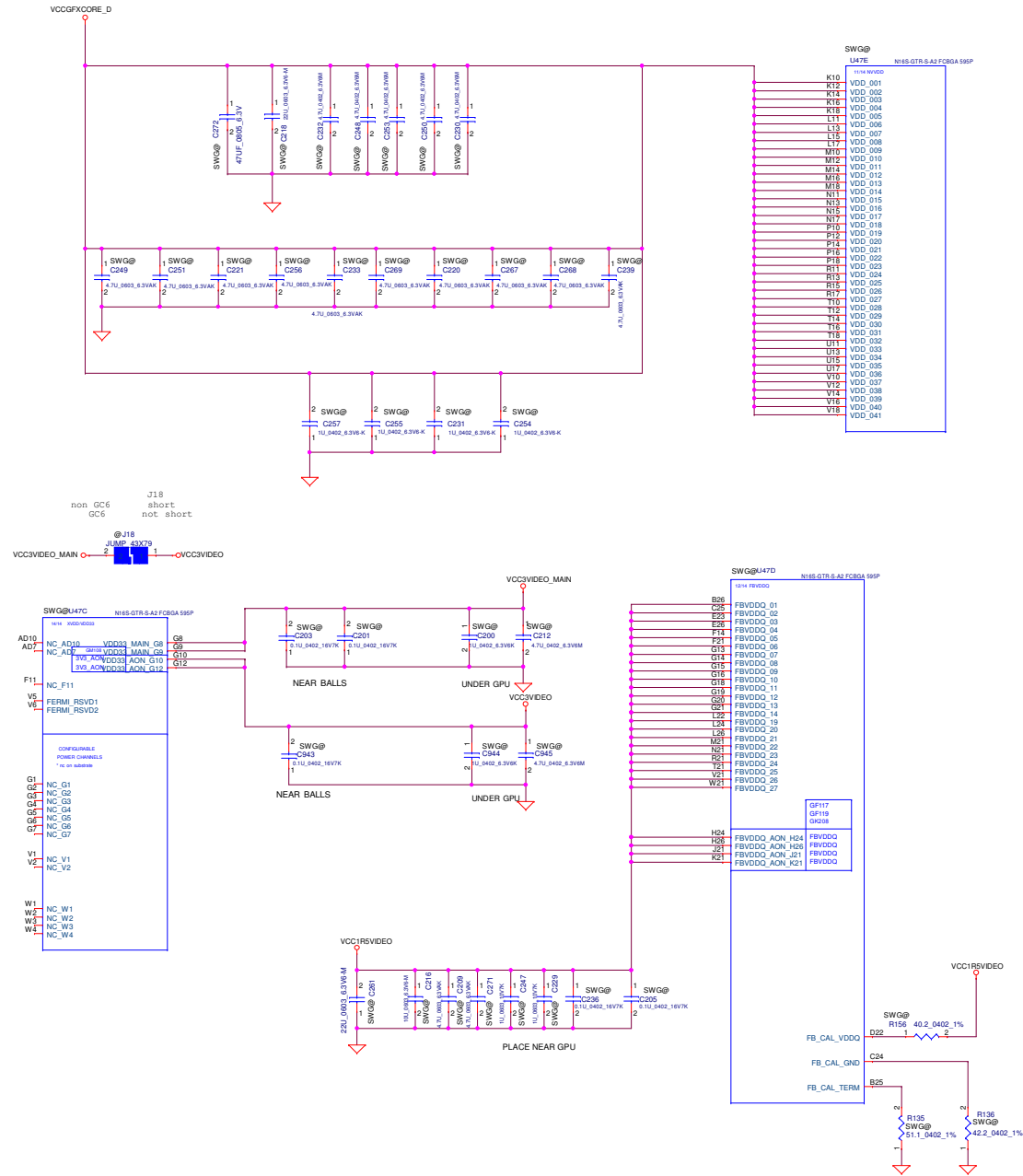
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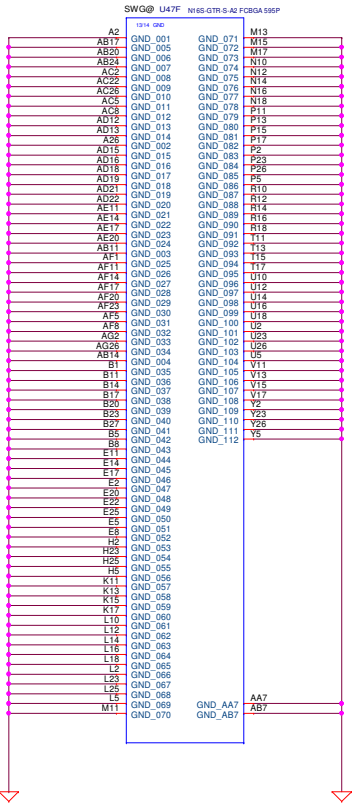
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				Date:	Thursday, October 15, 2015
				Sheet	27 of 97
				Rev	0.1

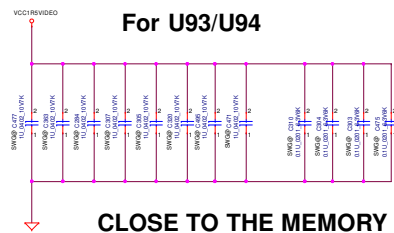




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		2012/06/21		N16S-GTR(3/6) VRAM I/F	
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Date		Thursday, October 15, 2015		0.1	
Sheet		30		of 97	



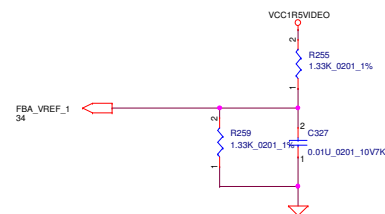
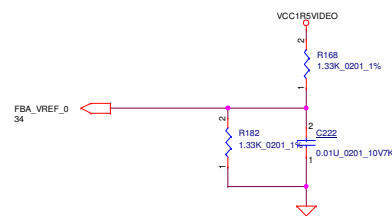



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Size	Document Number	COBAIN SWG			Rev
Quoted	Date: Thursday, October 15, 2015			Sheet	35 of 97





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Size	Document Number	Rev	
Custom		0.1	
Date:	Thursday, October 15, 2015	Sheet	36 of 97

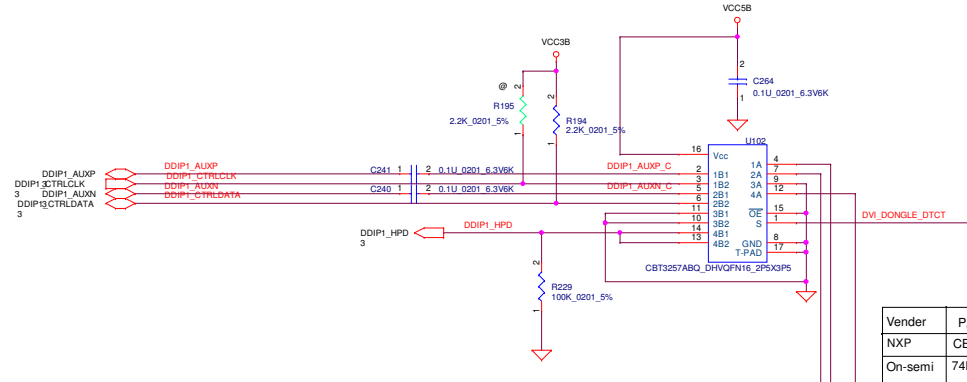
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AR U58

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				Date:	Thursday, October 15, 2015 15:58 37 of 87

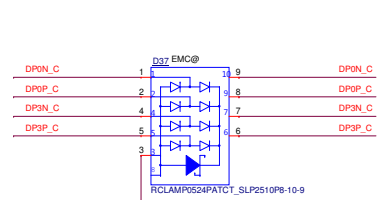
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Size	Document Number	COBAIN SWC			Rev
Custom					0.1
Date:		Thursday, October 15, 2015		Sheet 99 of 97	

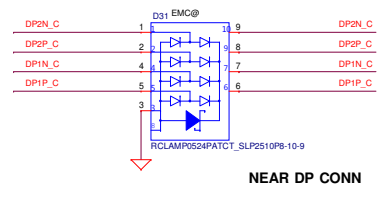


Vender	P/N
NXP	CBT3257ABQ
On-semi	74FST3257MNTWG

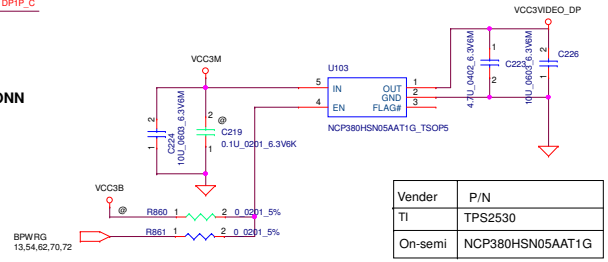
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BDIP1_3P	C319	1	2	0.1U_0201_6.3V6K	DP3P_C
DDIP1_2N	C263	1	2	0.1U_0201_6.3V6K	DP2N_C
BDIP1_2P	C265	1	2	0.1U_0201_6.3V6K	DP2P_C
DDIP1_1N	C266	1	2	0.1U_0201_6.3V6K	DP1N_C
BDIP1_1P	C276	1	2	0.1U_0201_6.3V6K	DP1P_C
DDIP1_0N	C280	1	2	0.1U_0201_6.3V6K	DP0N_C
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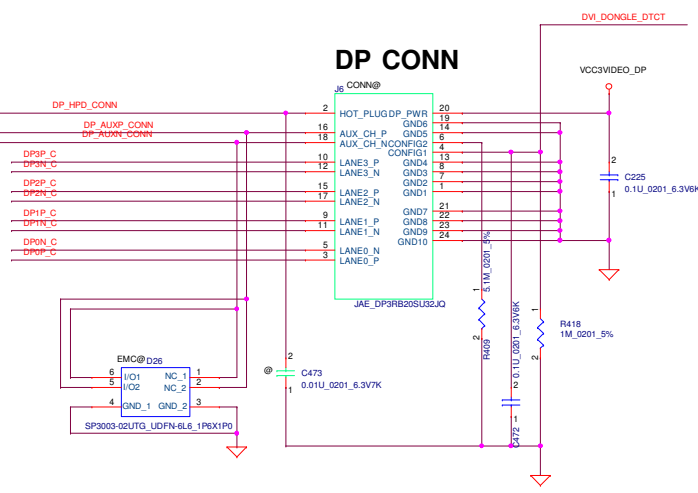
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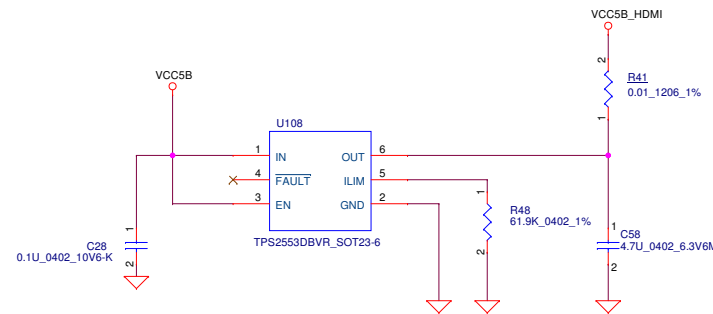
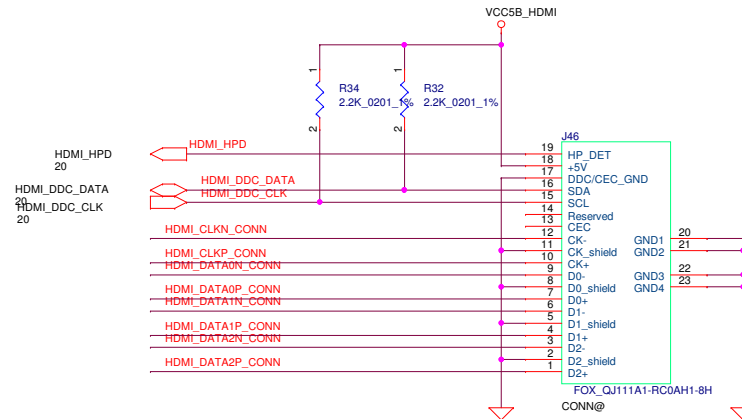
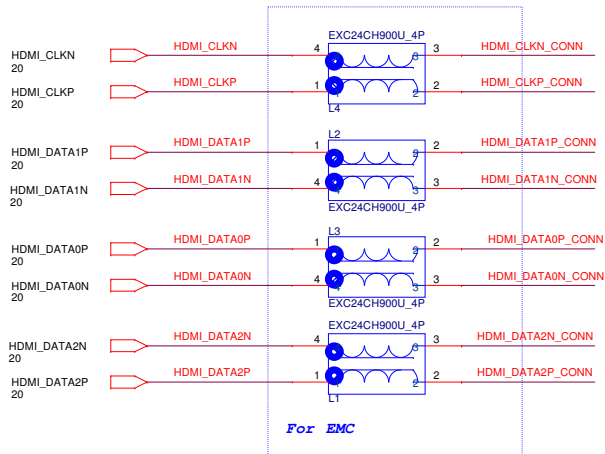
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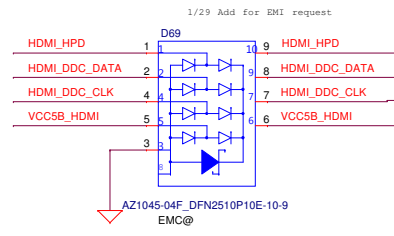
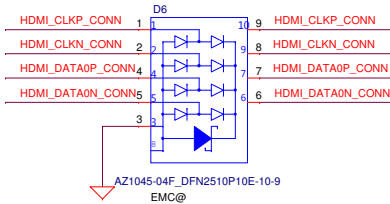
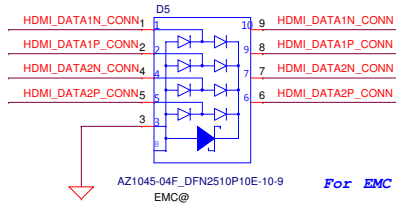
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TI	TPS2530
On-semi	NCP380HSN05AAT1G



DP CONN



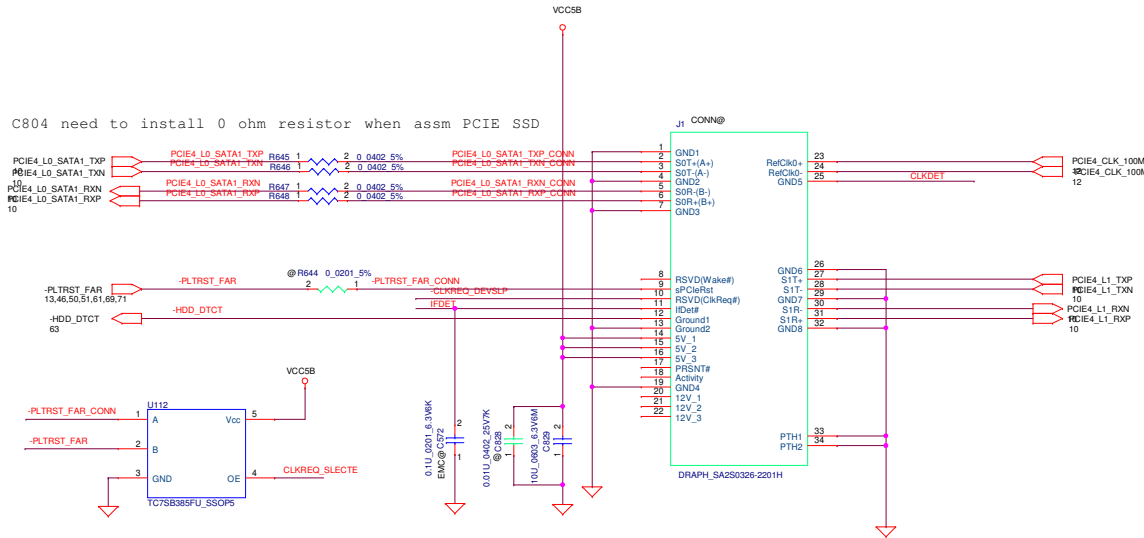
Close to J46



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Issued Date	2013/08/08	Deciphered Date	2013/08/05
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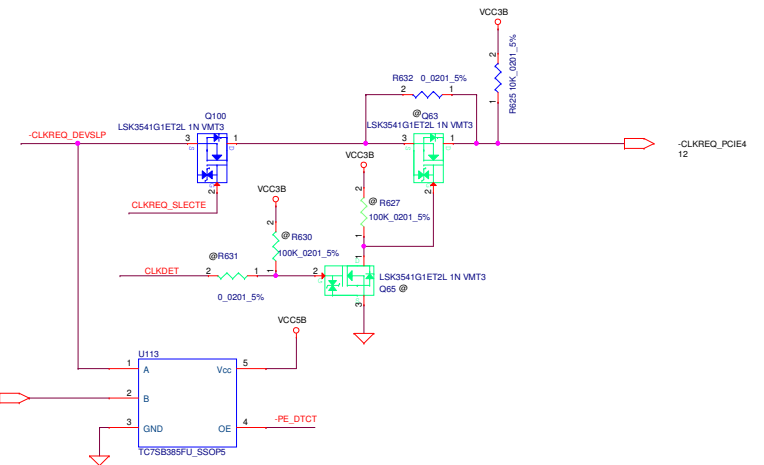
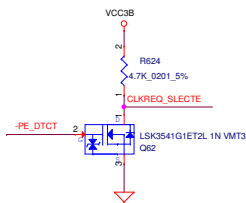
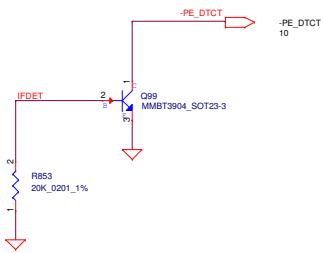
Title		LCFC	
HDMI CONN			
Size	Document Number	COBA1N3	
Custom			
Date:	Thursday, October 15, 2015	Sheet	42 of 97
Rev	0.1		


C803 and C804 need to install 0 ohm resistor when assm PCIe SSD



IFDET
SATA Device
PCIe Device

GND
5K PU to Vsource



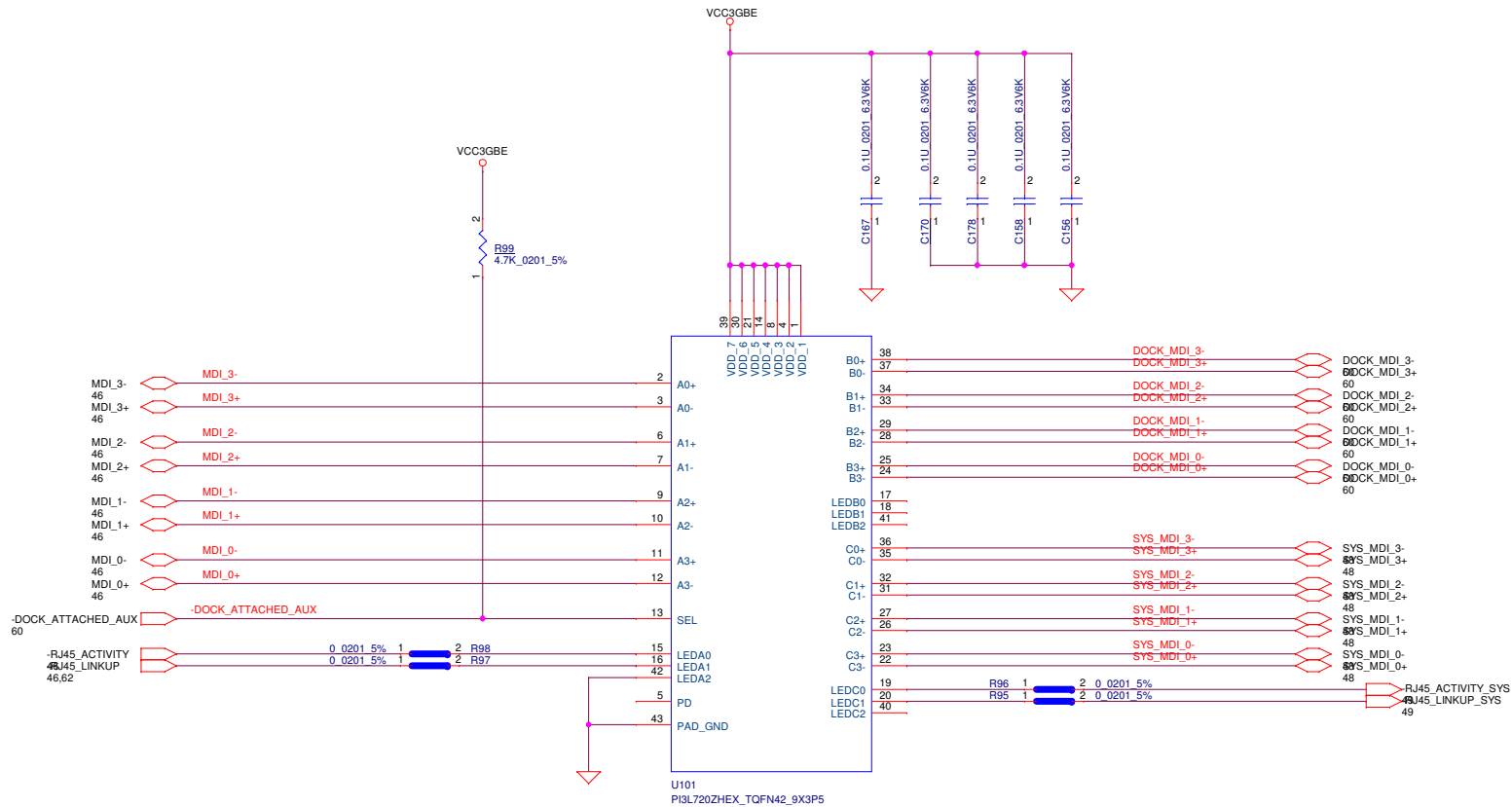
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Issued Date		2012/06/21		Deciphered Date		2012/06/21		SATA HDD CONN			
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								Document Number		0.1	
								Date		Thursday, October 15, 2015	
								Sheet		43 of 97	

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Issued Date	2012/05/02	Deciphered Date	2012/5/02	BLANK	
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				Date:	Thursday, October 15, 2015
				Sheet	44 of 97
				Rev	0.1



COBAIN SWG



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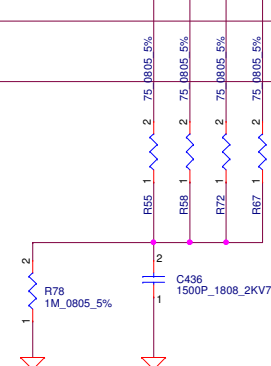
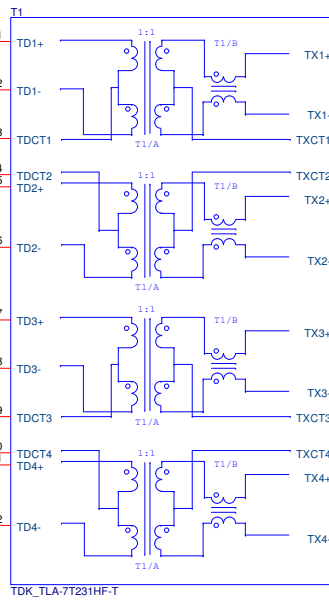
Vendor	P/N
Pericom ST micro Onsemi TI	PI3L720ZHE STMUX1800E NCH7201 TS3L501E

THE WIDTH OF THESE TRACE SHOULD BE WIDER THAN 35MIL TO PREVENT VOLTAGE DROP.

C303 SHOULD BE PLACED AS CLOSE TO MAGNETICS AS POSSIBLE.

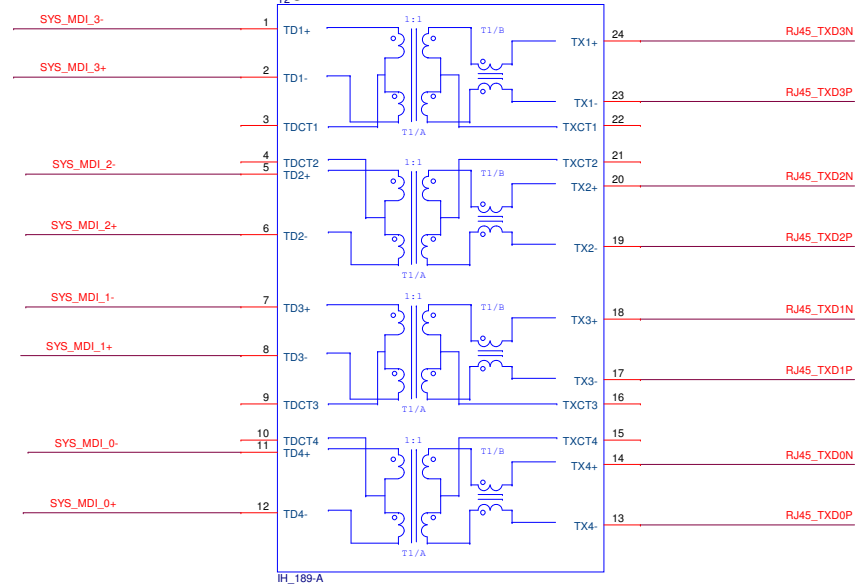
ESD REASON

Vendor	P/N
TDK	TLA-7T231HF-T
Timag	IH-115-F
Bothand	NA69LF



PATTERN MUST BE SHORT AND WIDE.

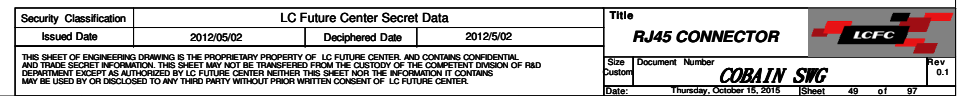
HIGH VOLTAGE 1500PF CAP IS OPTIONAL



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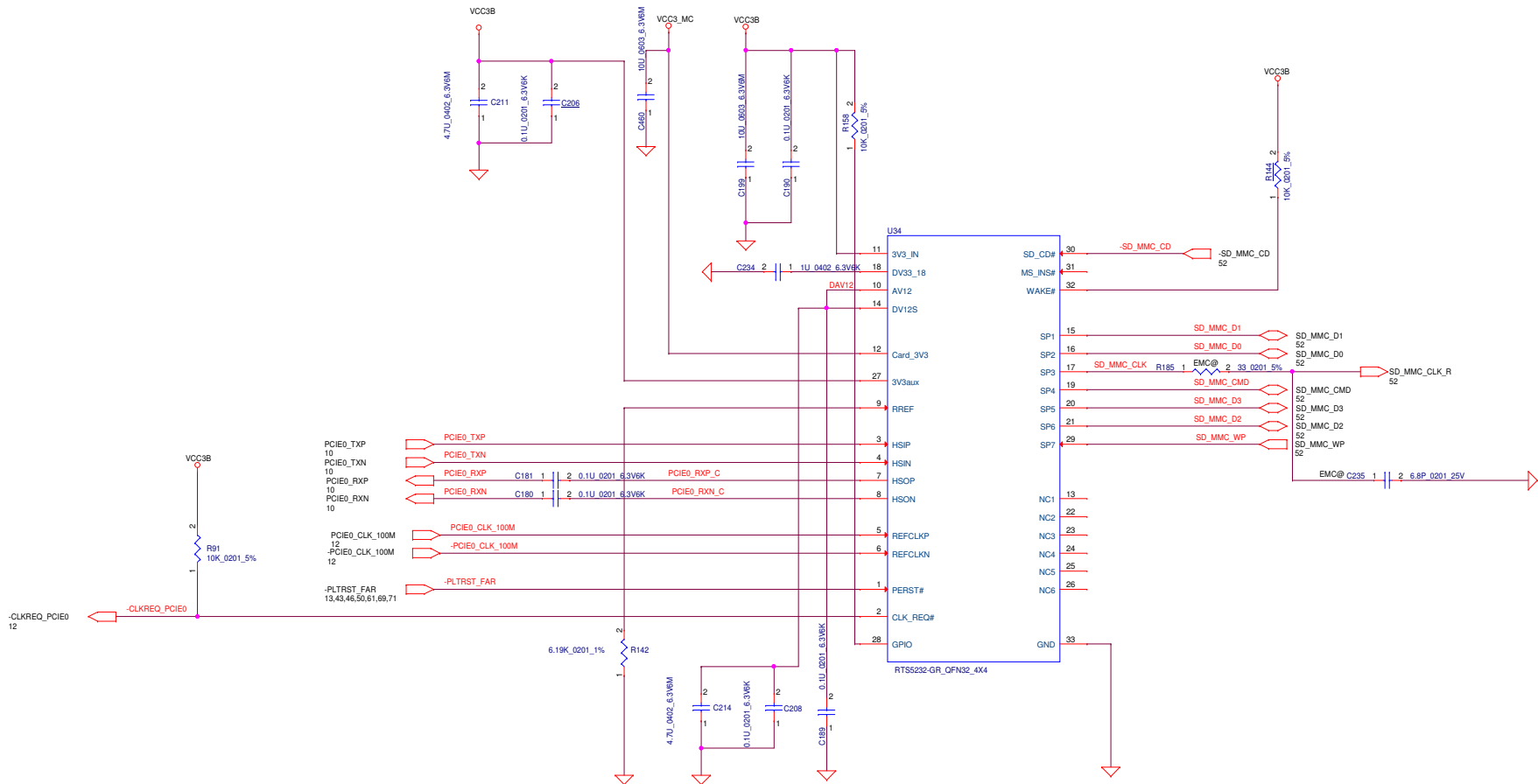
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GBE MAGNETICS		
Size	Document Number	Rev
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Date:	Thursday, October 15, 2015	Sheet 48 of 97

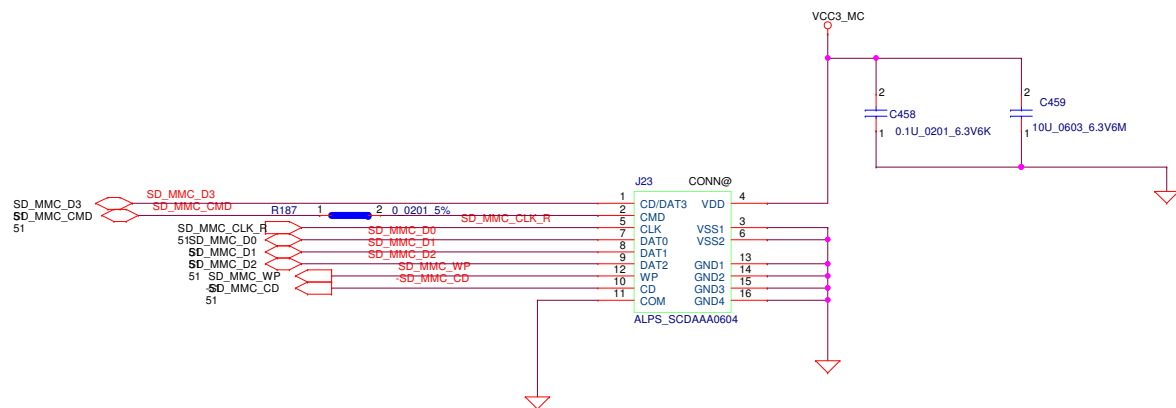





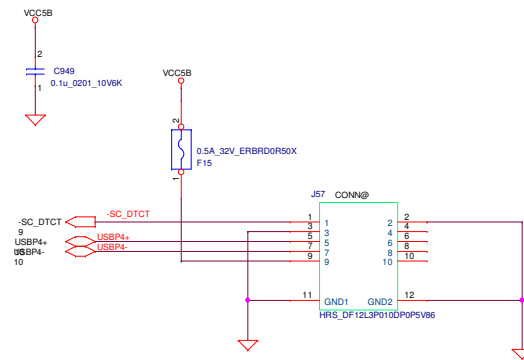
3.2H CONNECTOR




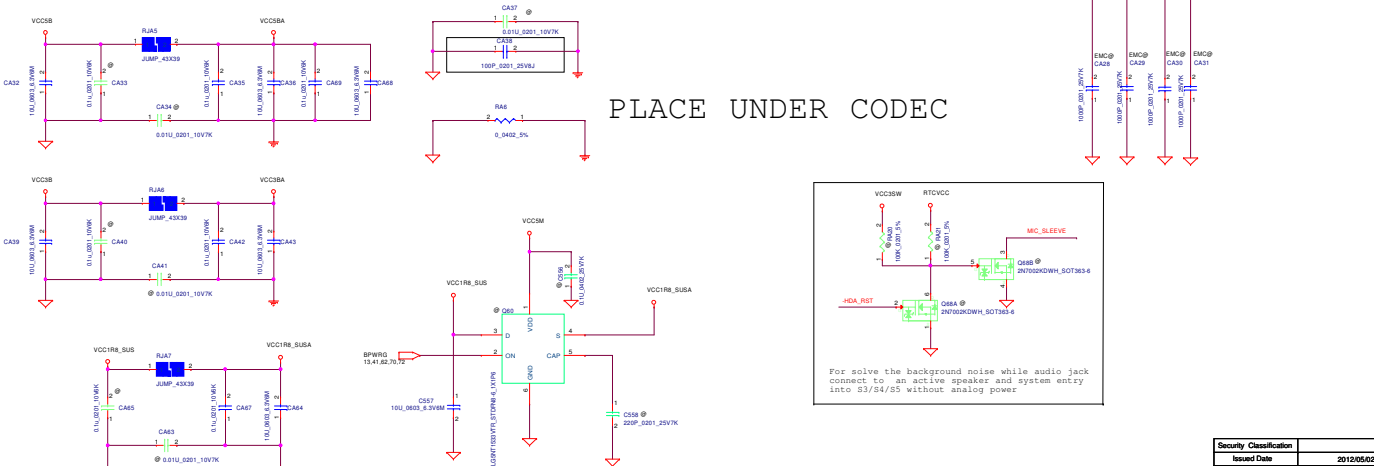




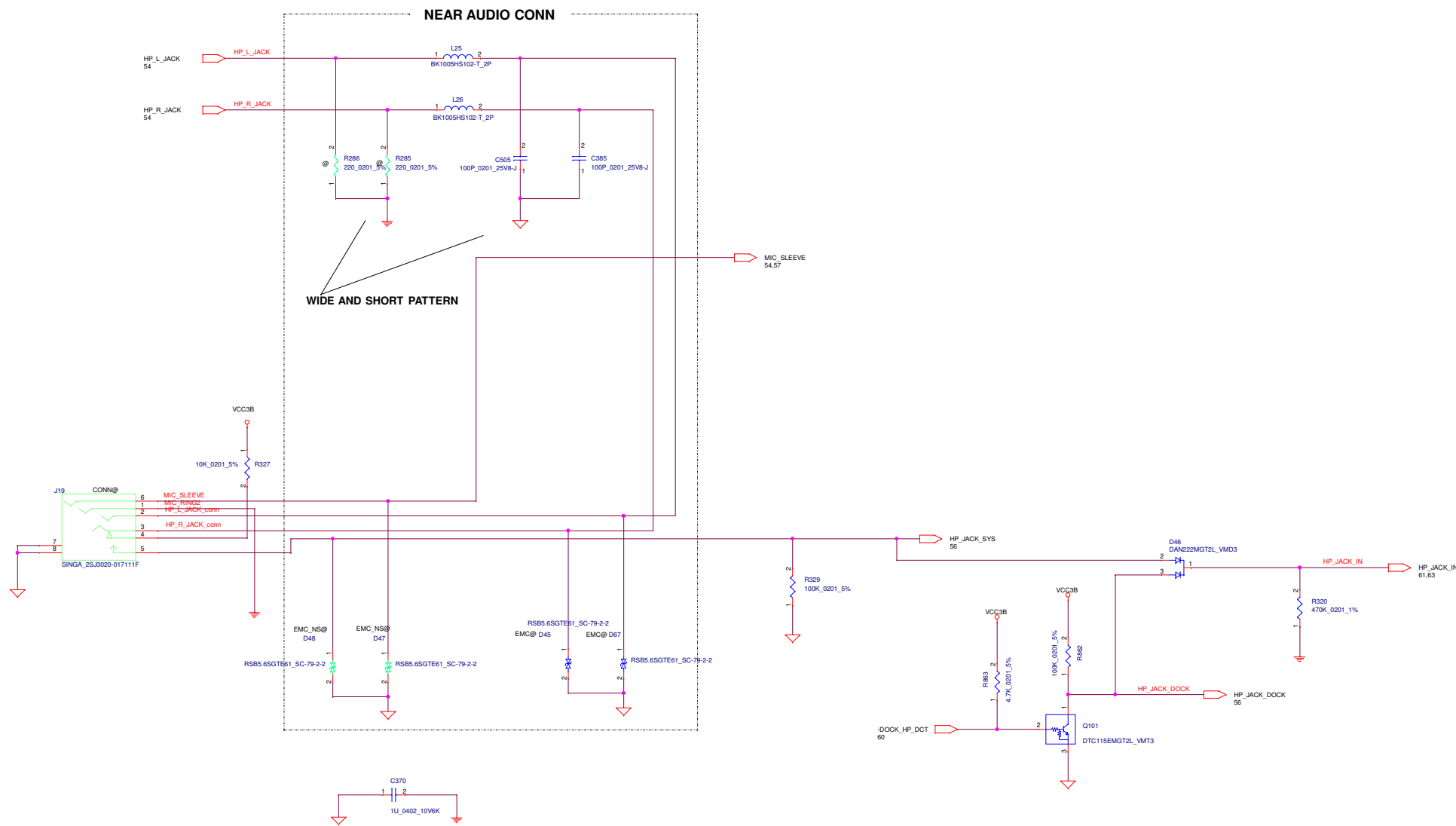
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				Date:	Thursday, October 15, 2015	Sheet	52 of 97

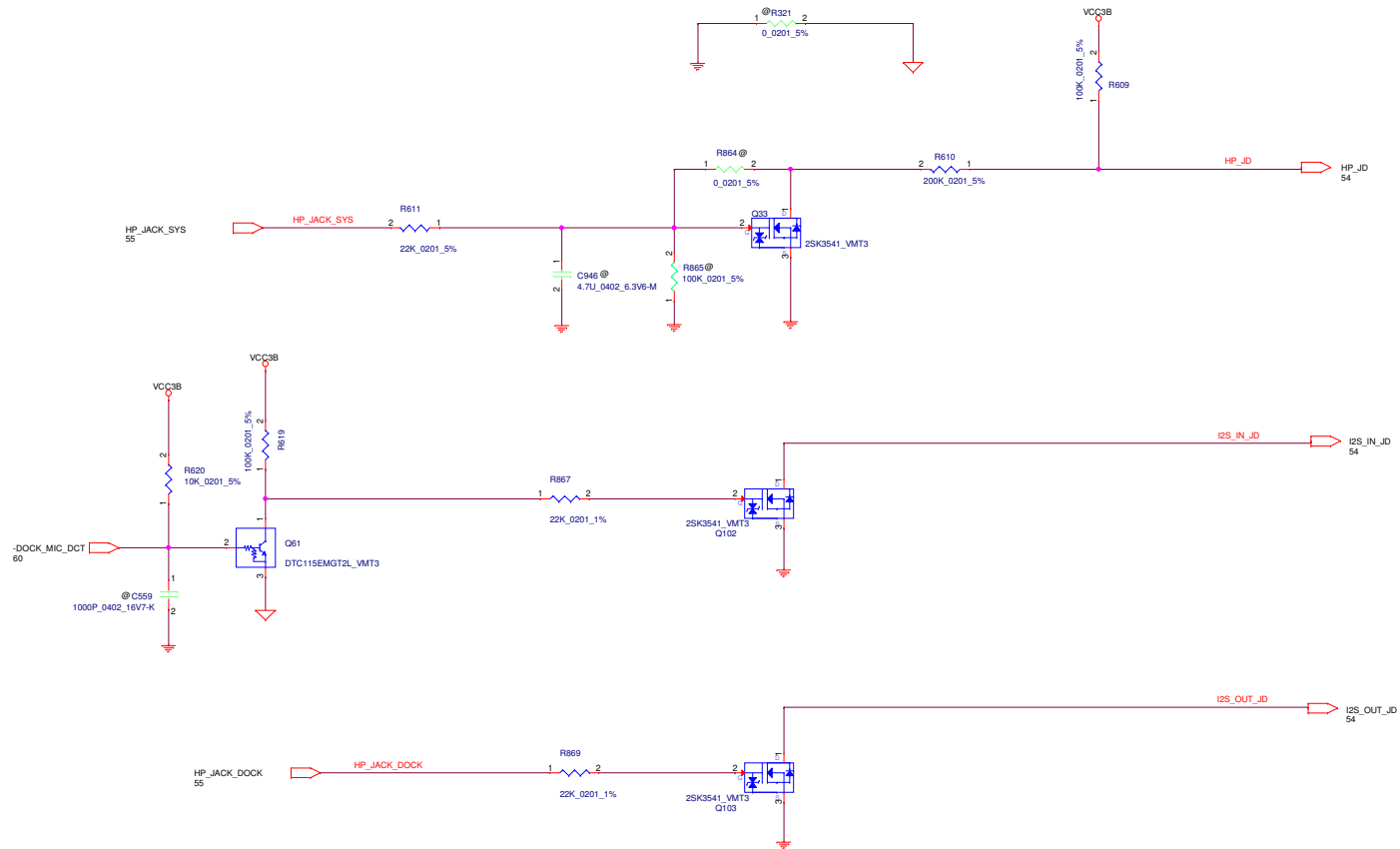


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Issued Date	2012/07/01	Deciphered Date	2014/07/01	SMART CARD I/F			
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Size	Document	Number	Revision		Rev		
Challin	COBAIN3		0.1				
Date:	Thursday, October 15, 2015		Sheet	53	of	97	

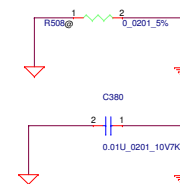
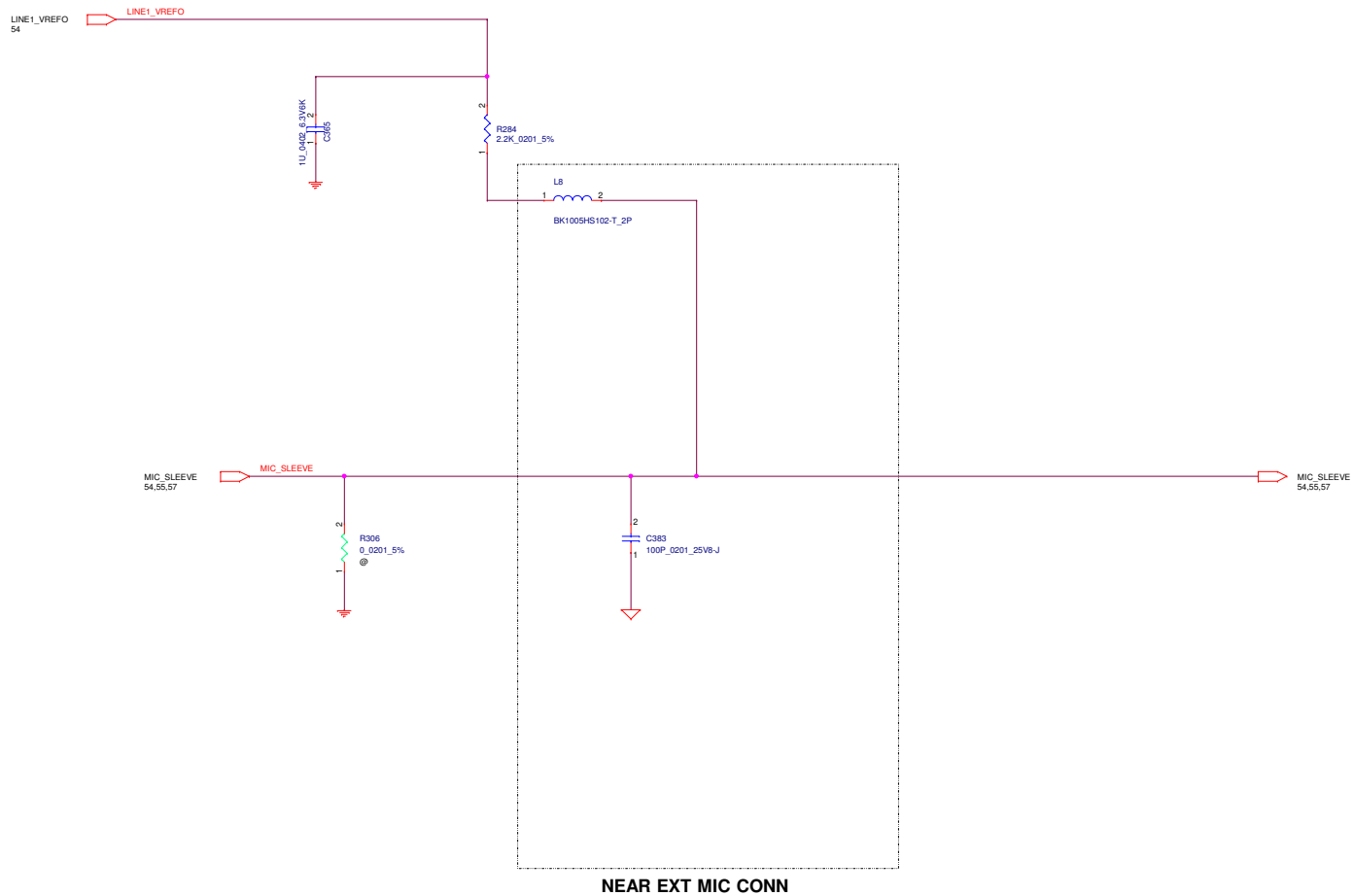


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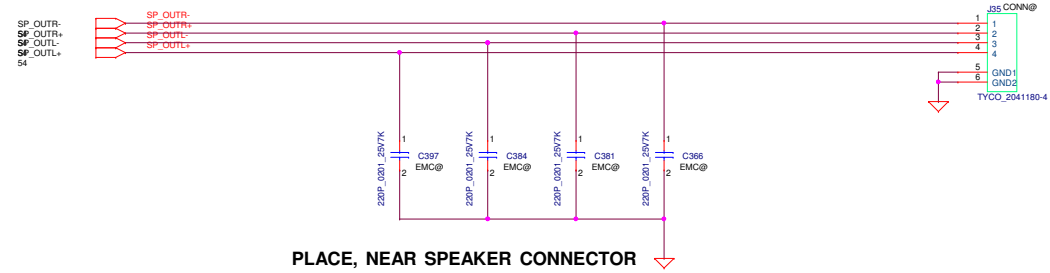
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Issued Date		Deciphered Date		AUDIO JACK SENSE	
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Custom		C		COBATN3	
Date:		Thursday, October 16, 2015		Sheet 56 of 97	
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Size	Document Number	Rev		0.1	
Date:	Thursday, October 15, 2015	Sheet	57	of	97

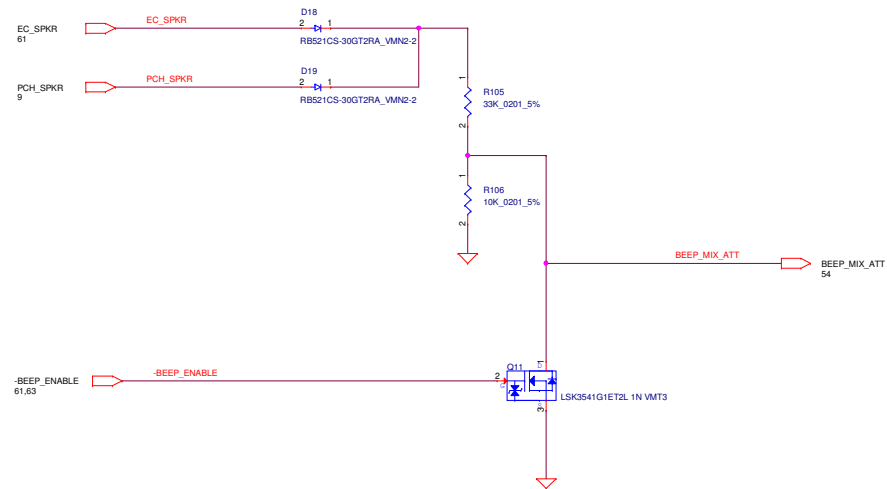


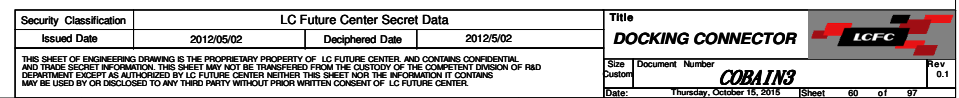
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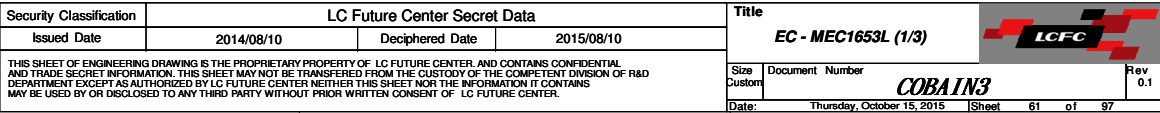


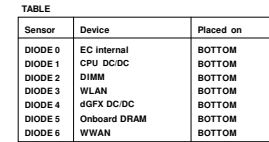
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				Date: Thursday, October 15, 2015	Rev 0.1
				Sheet 58 of 97	

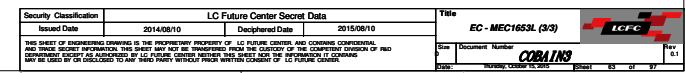


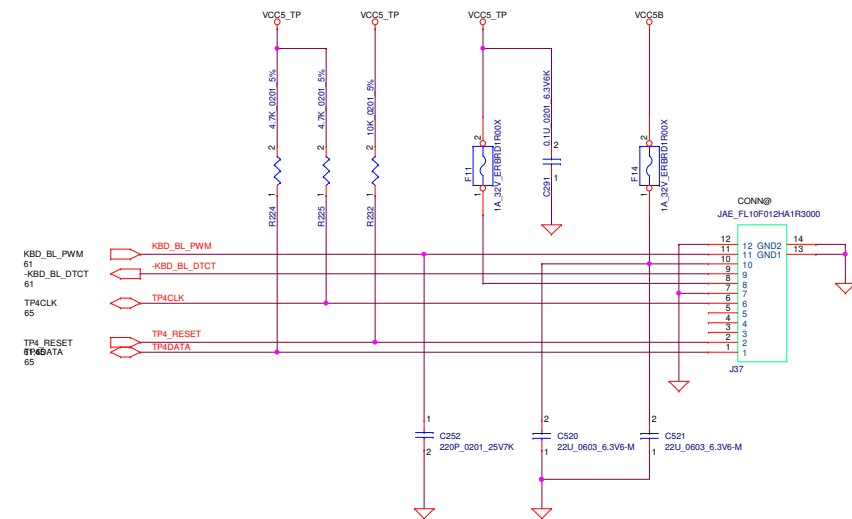






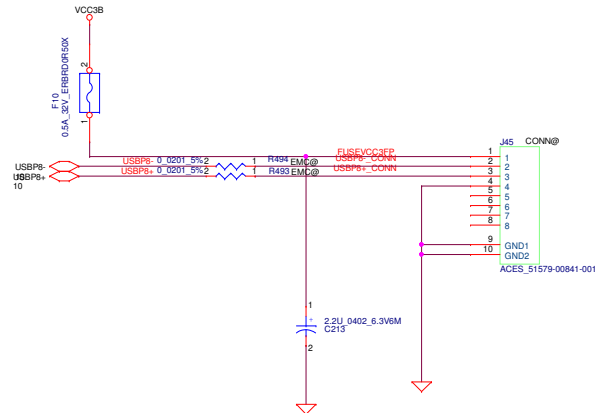
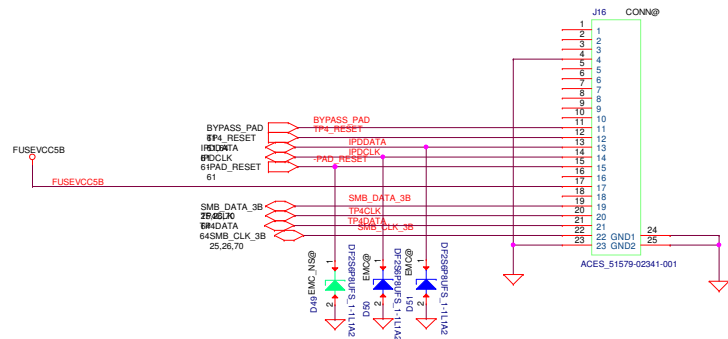
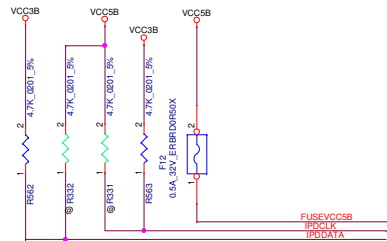








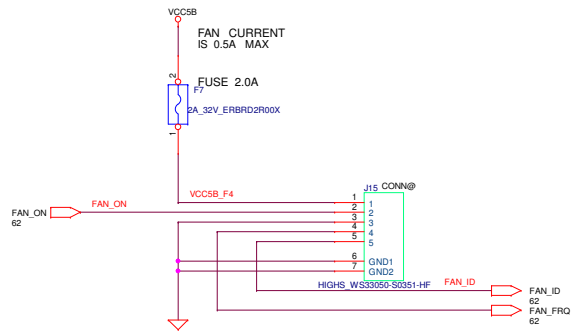
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Size		Document Number		Date				Rev			
Date		Thursday, October 16, 2015		Sheet		94		of		97	
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Size	Document Number			Rev	
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Date:	Thursday, October 15, 2015			Sheet 66 of 97	





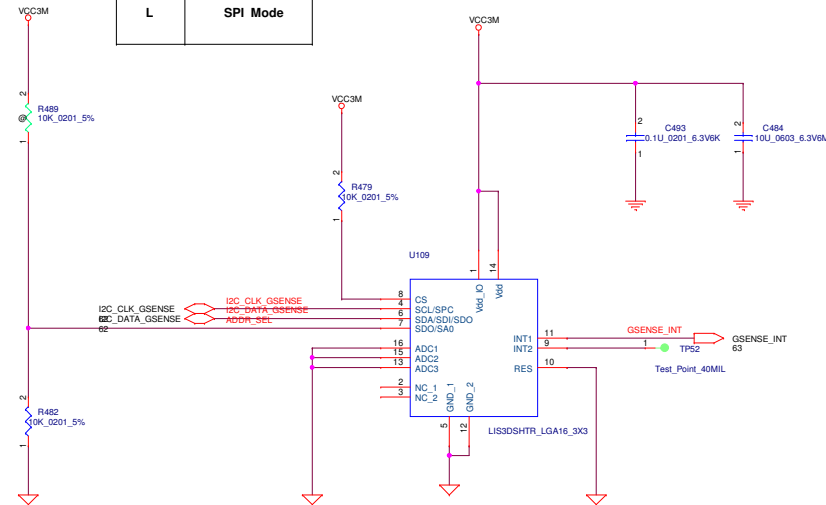
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Size	Document Number	COBAIN SWC		Rev	
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Date:	Thursday, October 15, 2015	Sheet	67	of	97


TABLE

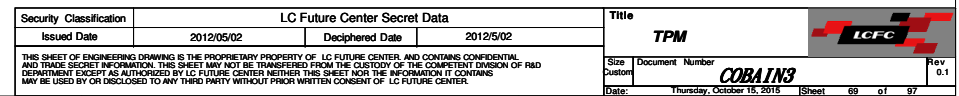
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KX023-1025	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)

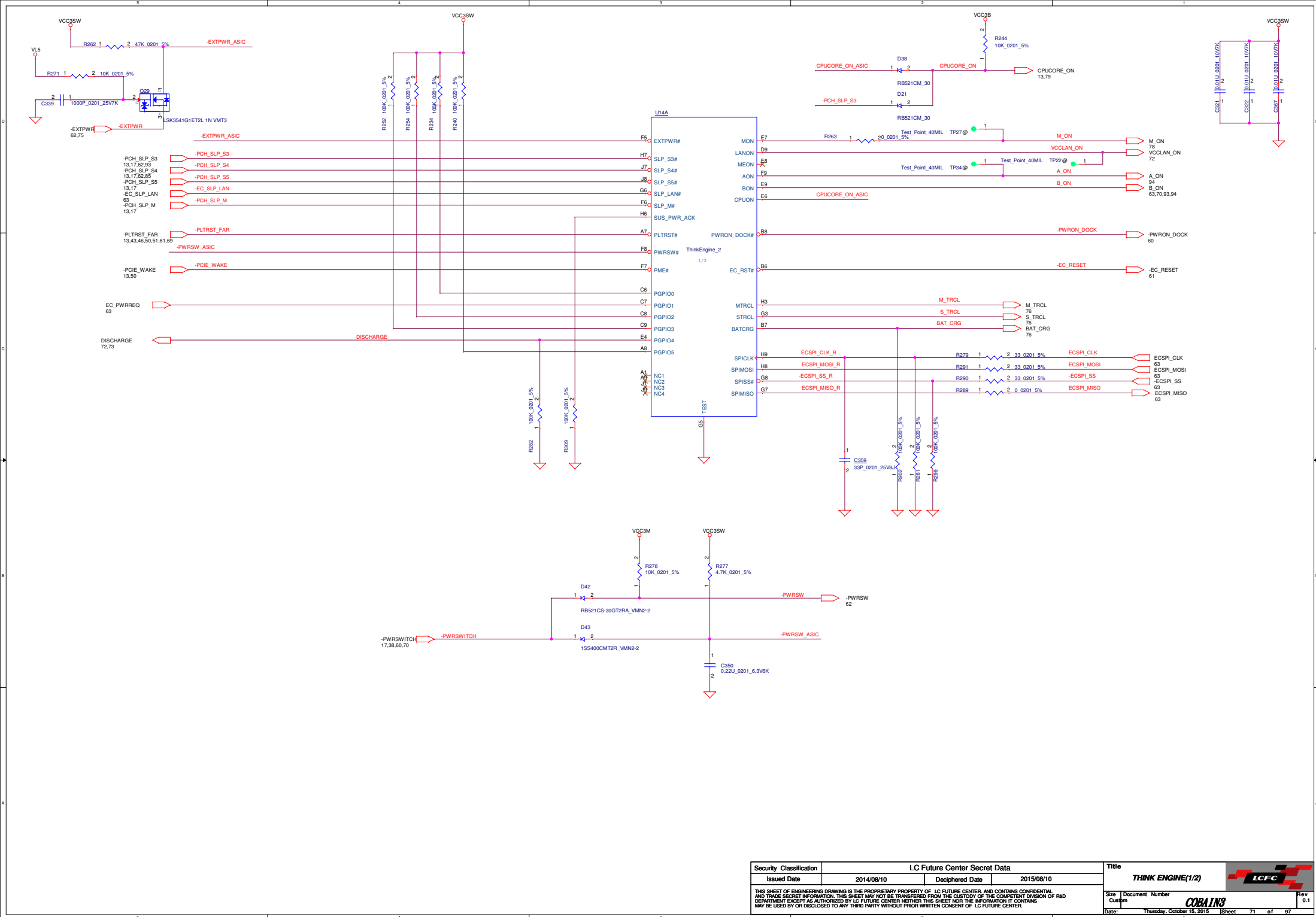
TABLE

P/N	Mode Selection
H	I2C Mode
L	SPI Mode



Security Classification		LC Future Center Secret Data		Title		
Issued Date		Deciphered Date		G-SENSOR		
2012/06/21		2012/06/21				
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Size		Document Number		Rev		
Custom		COBALT3		0.1		
Date:		Thursday, October 15, 2015		Sheet		68 of 97





DCIN

DOCK_PWR20

PLACE NEAR CONNECTOR

DCIN_PWR20_F

VINT20

Total MLCC capacitance at DCIN connector is smaller than 1000pF to avoid LC resonance

TABLE

PEAK SHIFT	YES	NO
RR10	NO-ASM	ASM
PR2	ASM	NO-ASM
PQ7	ASM	NO-ASM
PQ6	ASM	NO-ASM

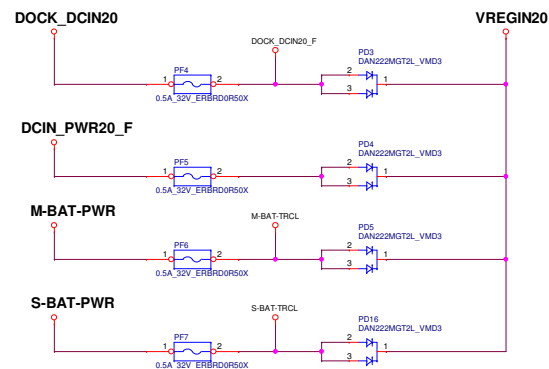
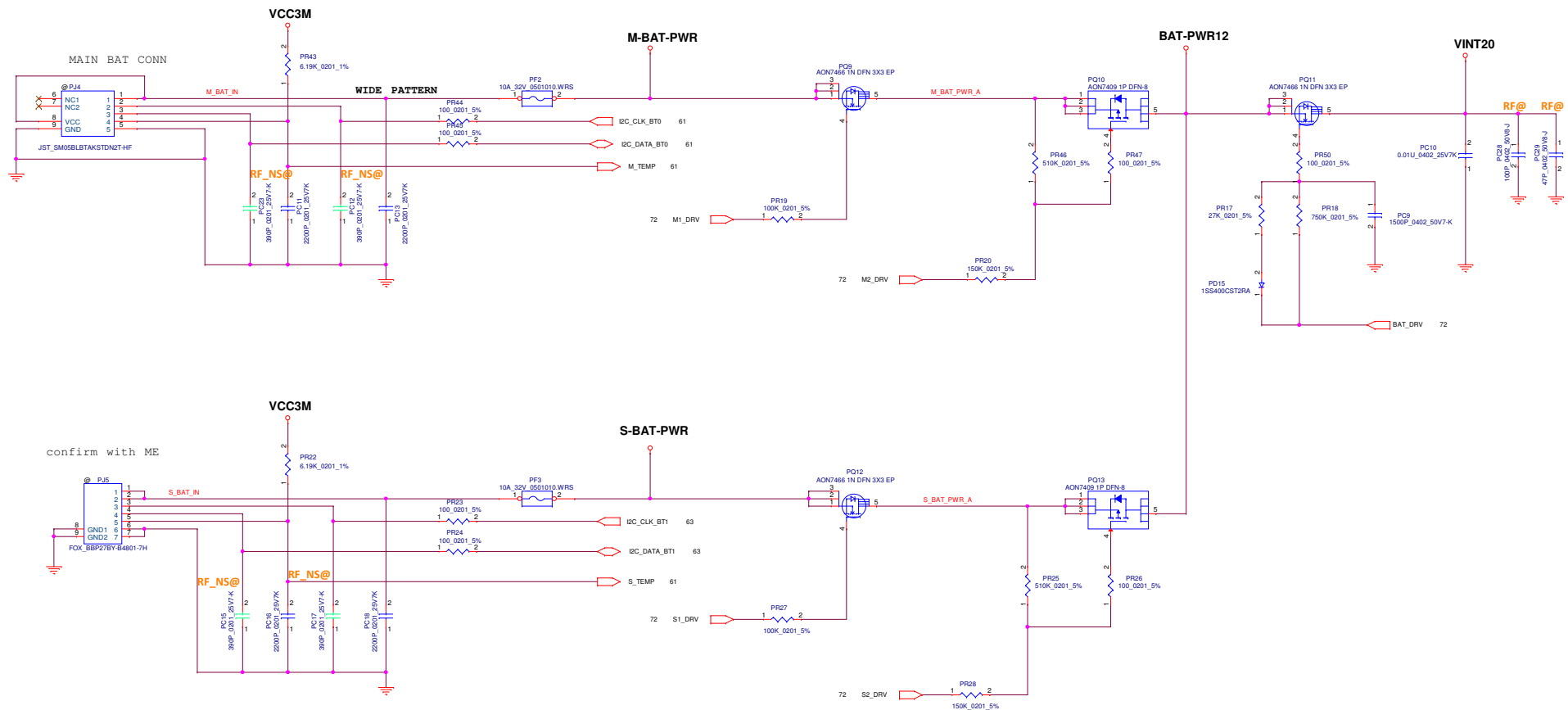
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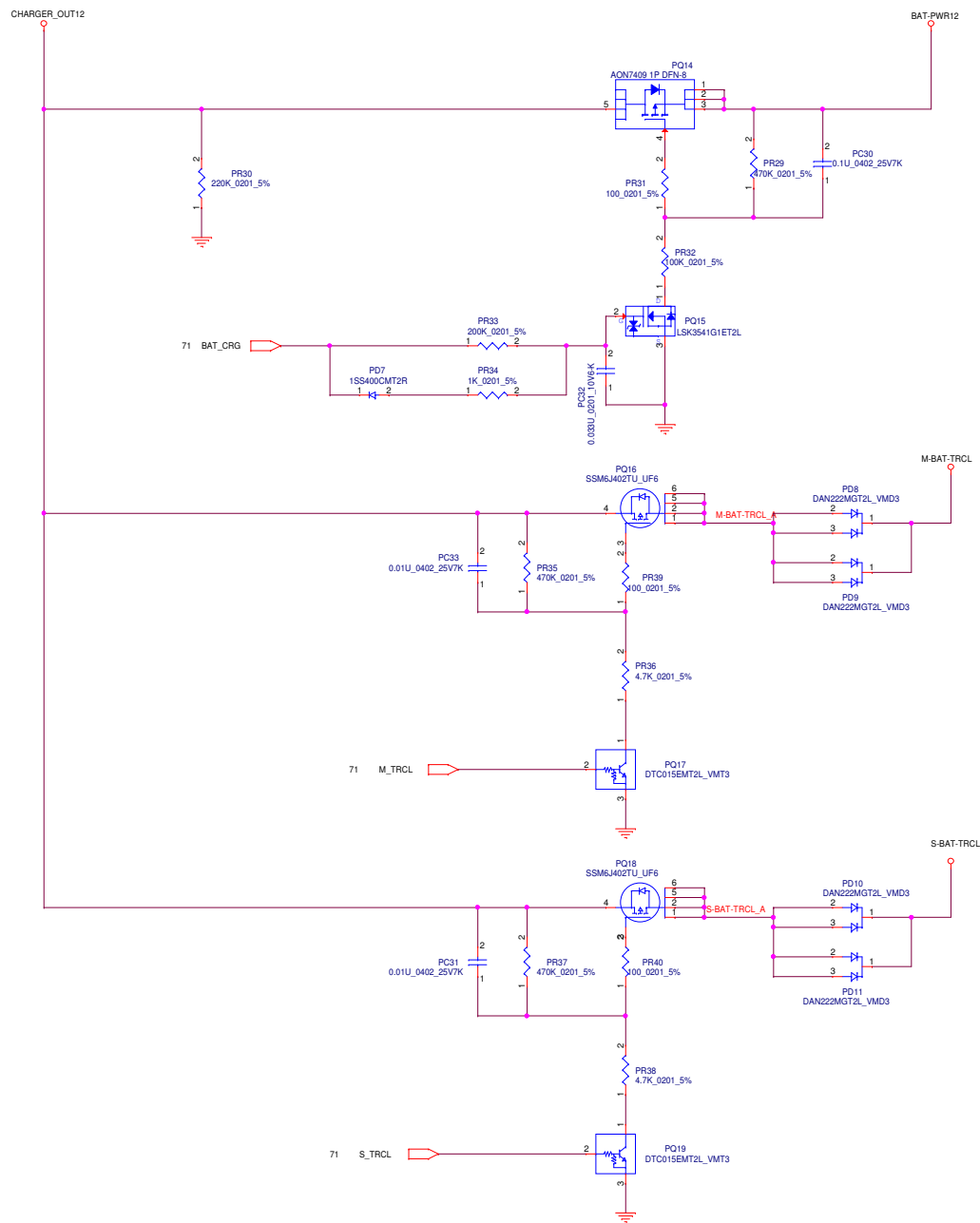
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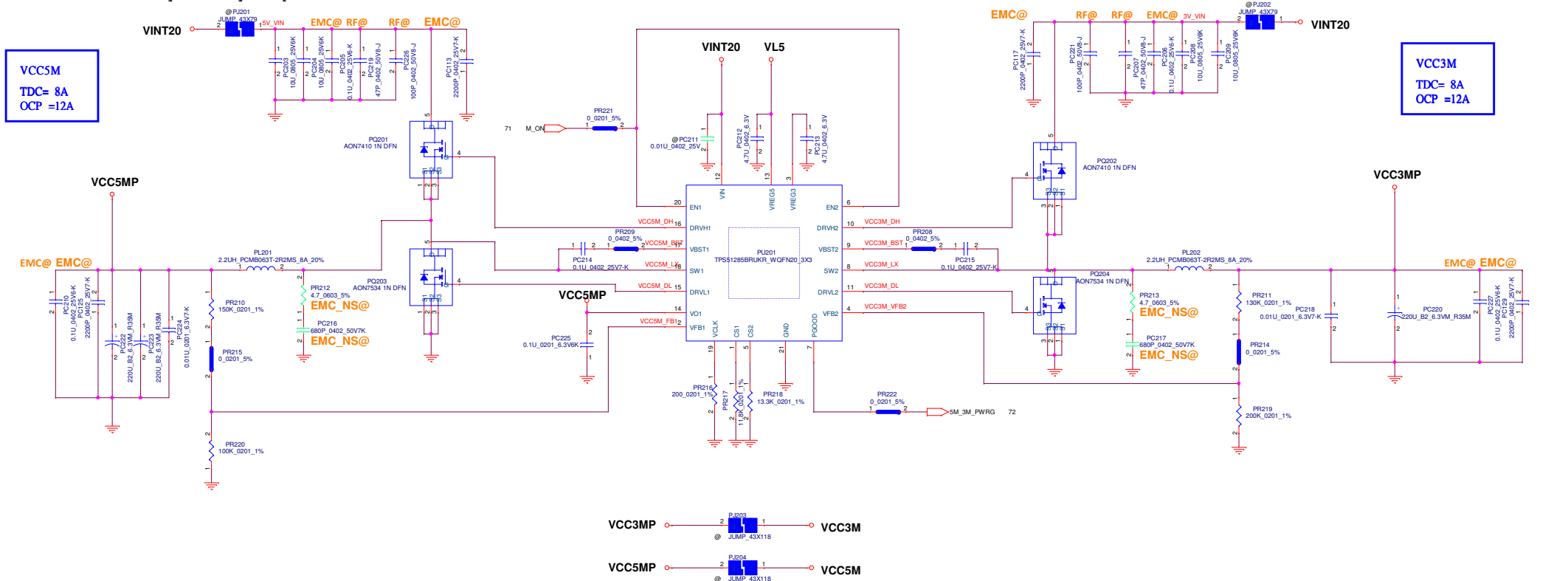
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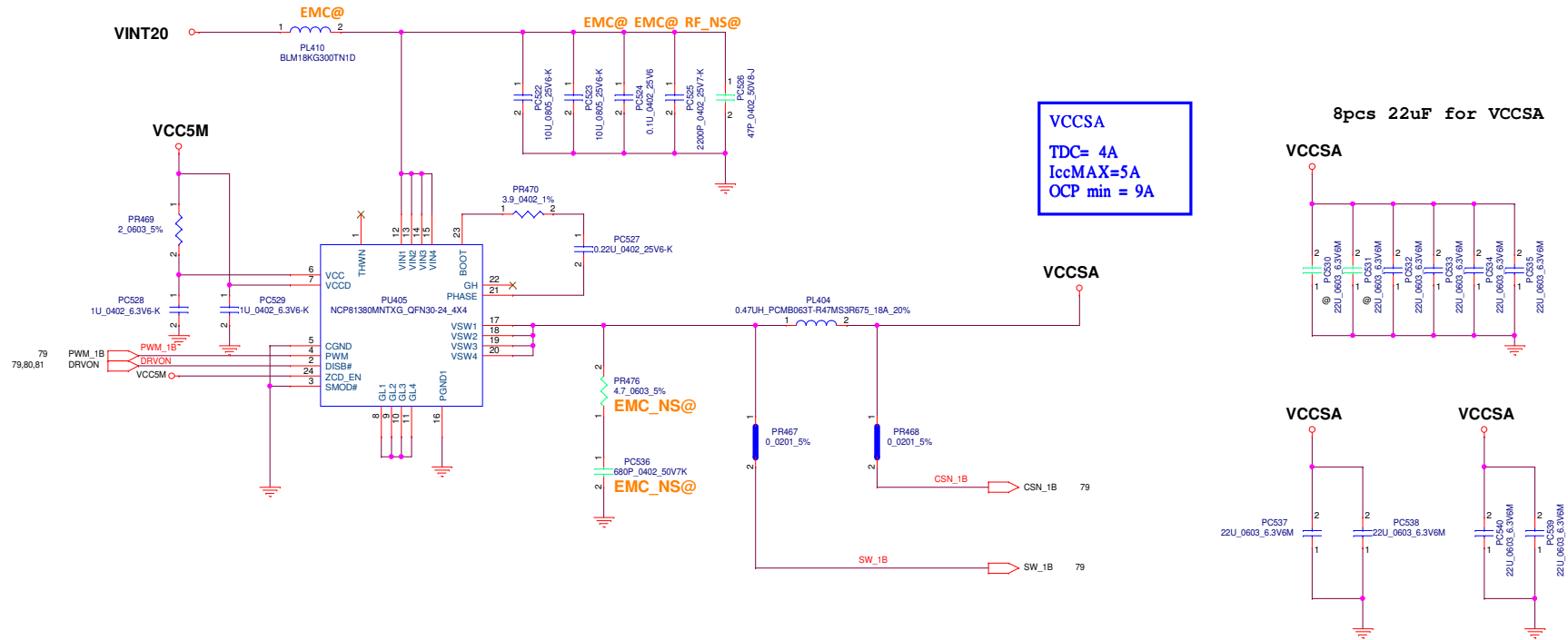
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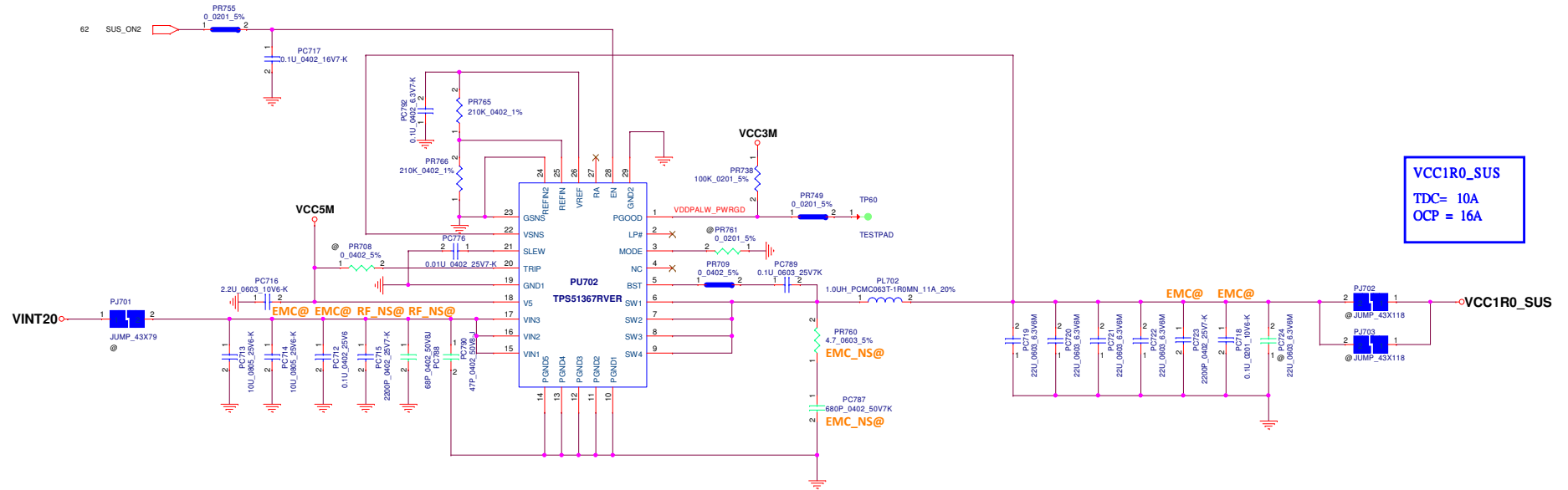
All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.




All the input MLCCs must be placed symmetrically on Top and Bottom.



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Date:	Thursday, October 15, 2015	Sheet	82	of	95




Mode	Frequency
GND	400KHz
Float	800KHz

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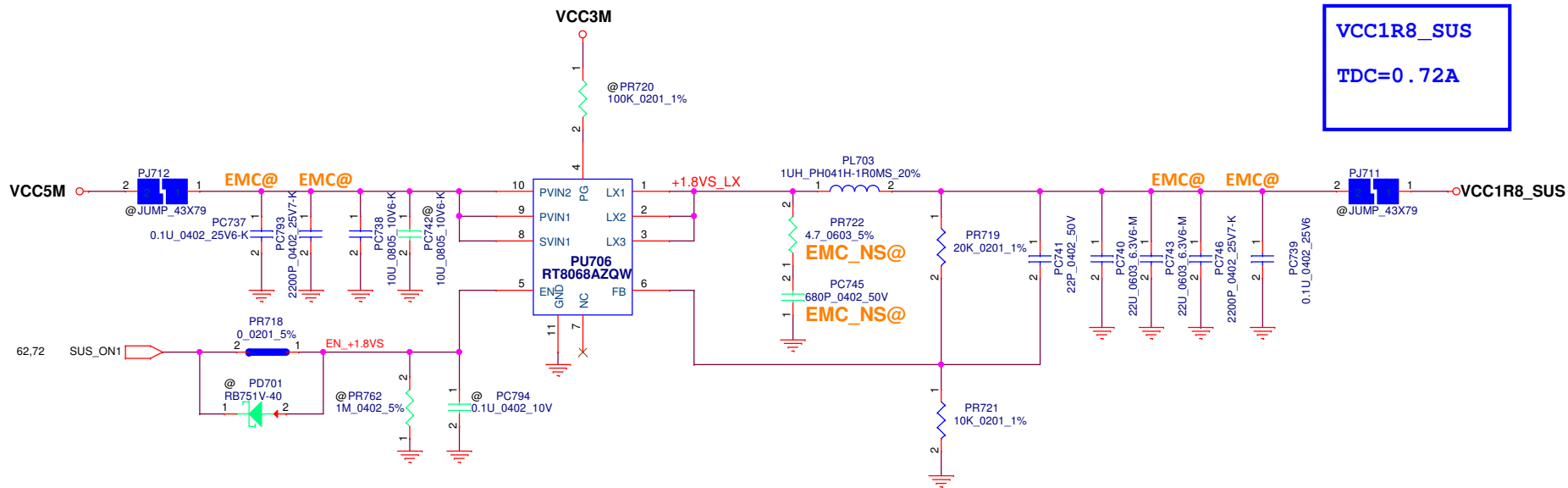
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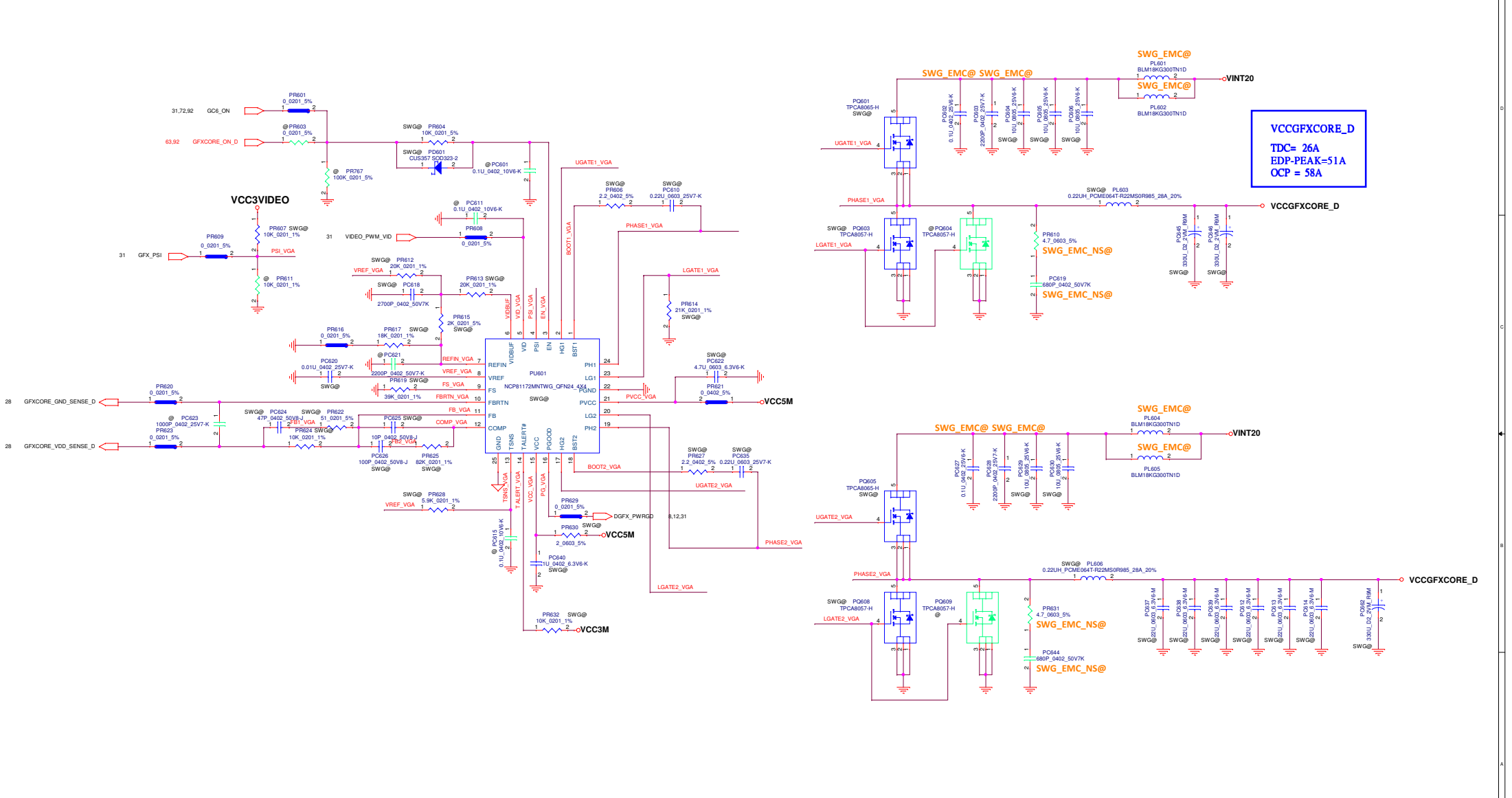


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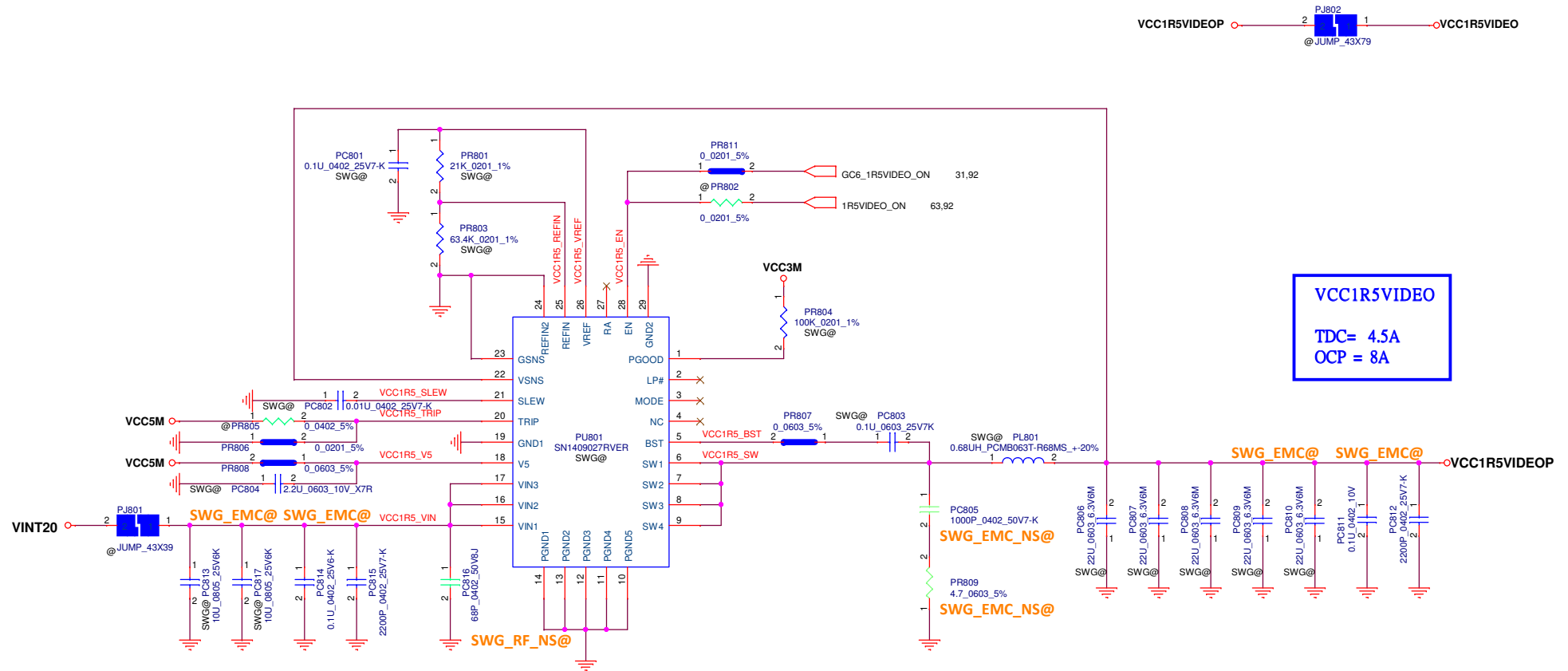
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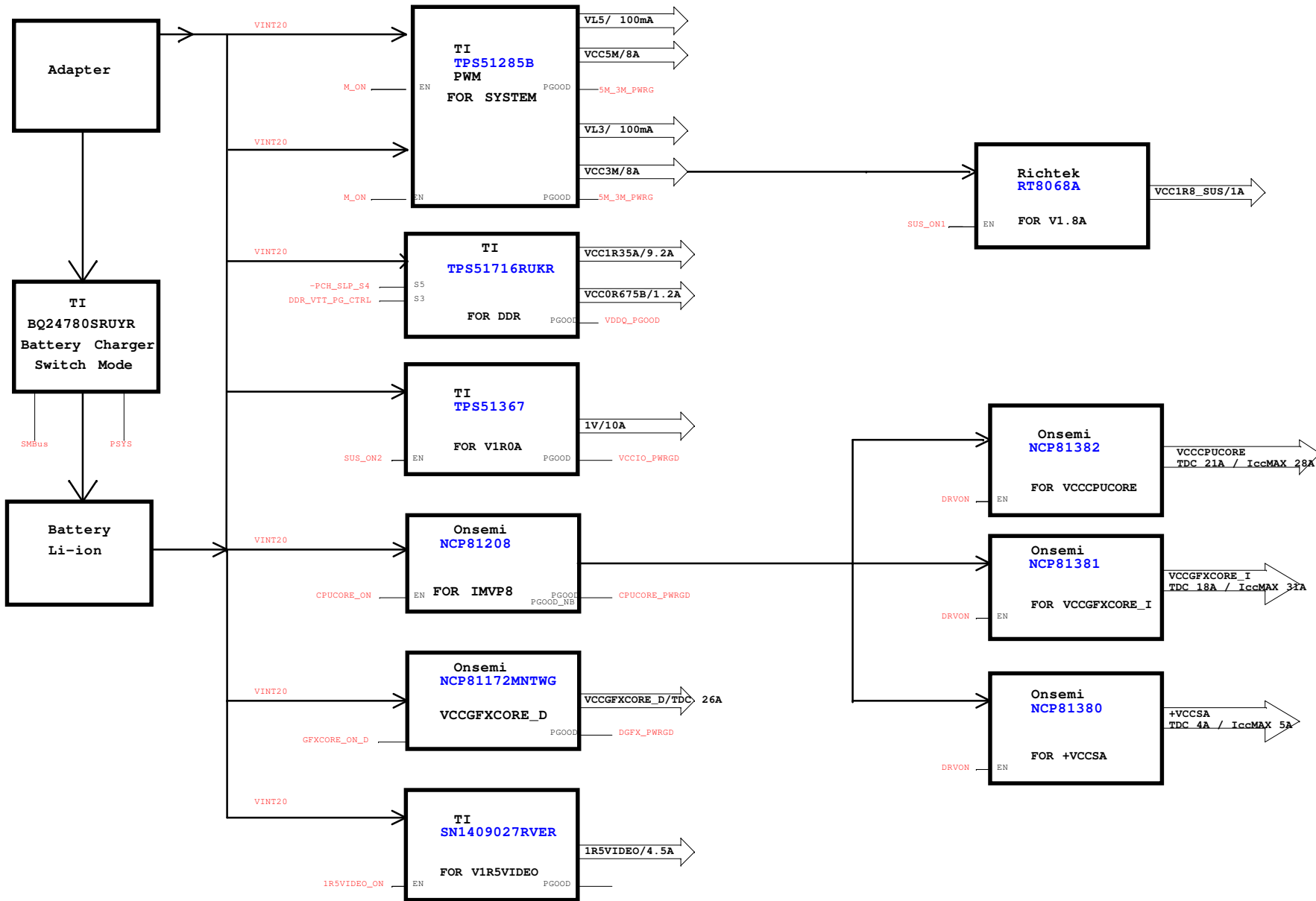
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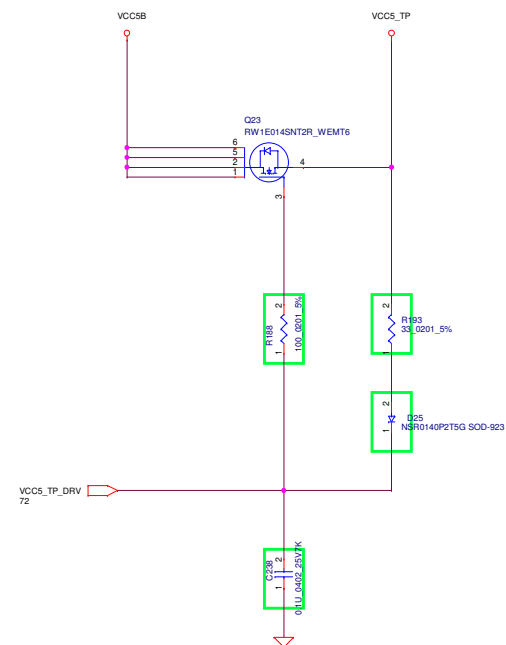





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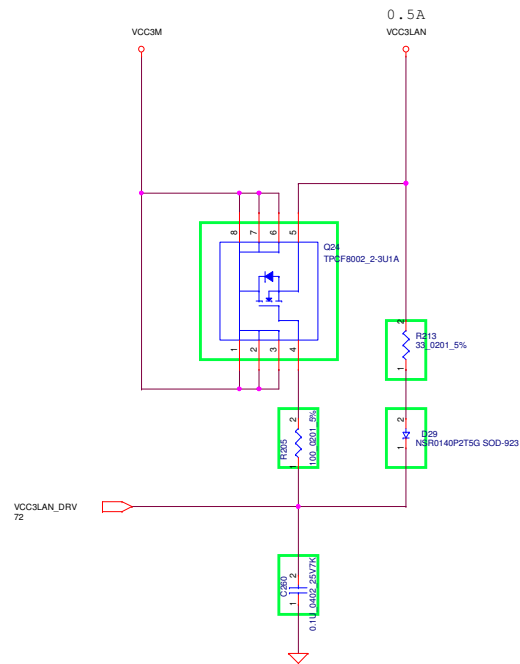


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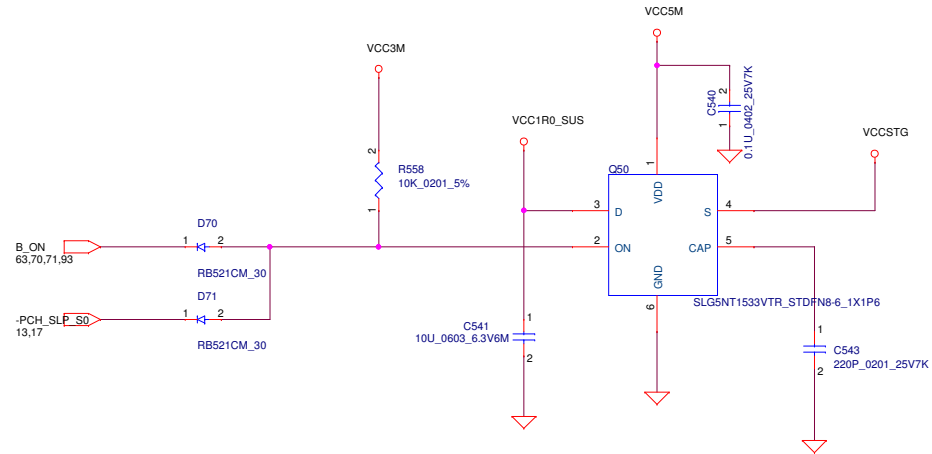
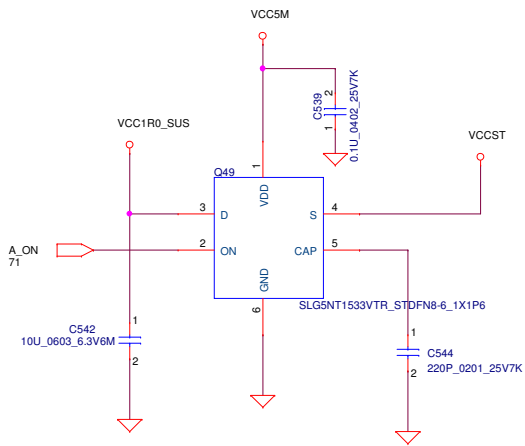



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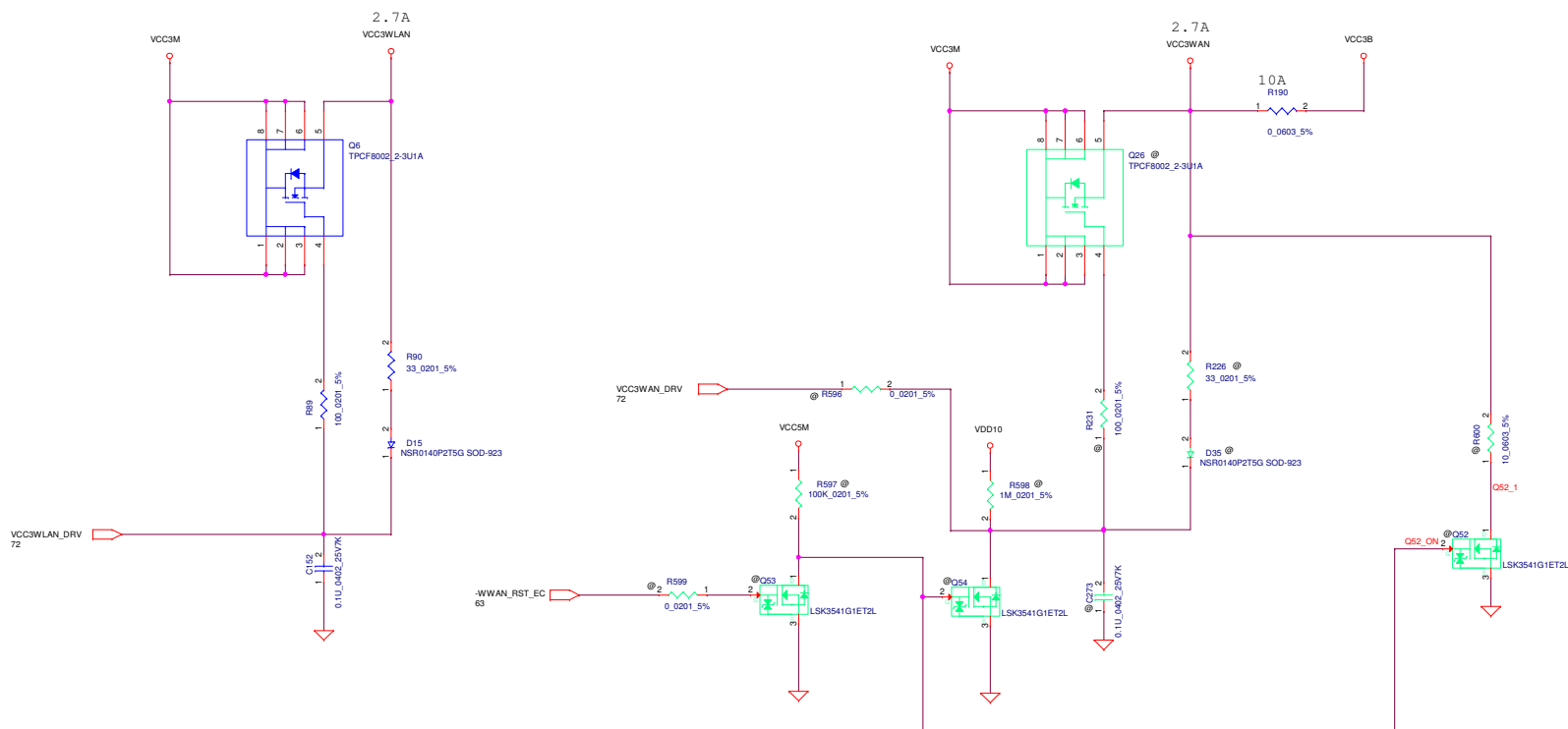



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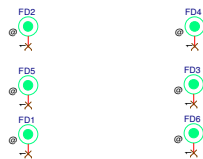
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Component	Area

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